MARCO IFC/C2S2/GSRC Workshop

Chip-Scale Power Scaling:
*How to get the current in and the heat out?*
*And how much power do we really need anyhow?*

Saturday, March 13, 2004
Packard Electrical Engineering Building, Room 101
Stanford University

**Agenda**

7:30   Breakfast
8:30   Welcome and introductions
9:00   Rajesh Kumar (Intel) “Understanding the Power Consumption in High Performance Microprocessors” (Keynote talk)
9:40   Larry Pileggi and Marija Ilic (Carnegie-Mellon) “Controlling the IC Power Grid,”
10:10  Break
11:00  Ravi Mahajan (Intel), “Cooling Challenges for Silicon Integrated Circuits”
11:30  Poster Preview
12:00  Lunch
       Posters on display
1:30   Ken Goodson (Stanford), “Advanced Cooling Technologies for Silicon Integrated Circuits”
2:15   Li-Shiuan Peh (Princeton) “Chip-Scale Networks: Power and Thermal Impact”
2:45   Break
3:15   Raul Camposano (Synopsys) “Power issues from a design methodology perspective” (tentative title)
3:45   Panel discussion
5:00   Reception

*Organized by the Center for Integrated Systems, Stanford University, in cooperation with Stanford Photonics Research Center*