



Linking Two Millennia

October 1999 marked the culmination of a more than 15-year process as the new David Packard Electrical Engineering building was officially opened and Stanford University celebrated the completion of the Science and Engineering Quad (SEQ).

The 70,000-square foot Packard building houses 27 faculty, 277 students, 36 staff, the Stanford Networking Research Center (SNRC), STAR Lab, and Information Systems Lab (ISL). It also has room to accommodate up to 71 visiting scholars and is slated to open an exhibit gallery in April, highlighting past faculty achievements and the ways they contributed to engineering and the growth of Silicon Valley. Located next door to the Gates building, CIS, and the historic Ginzton Lab, the Packard building is situated at the hub of the science and engineering community.

The completion of Packard signals more than the fulfillment of an ambitious construction project; it marks the beginning of an interdepartmental initiative leading Stanford, and engineering specifically, into the next millennium. The new structure reflects a spirit of renewal and expansion in Stanford's engineering community as a whole, where many changes have been realized in the past year, and still more linger on the horizon.

Some significant recent developments include the appointments of **John Hennessy** as Provost, **Jim Plummer** as the Dean of the School of Engineering, and **Bruce Wooley** as the new EE Chairman.



The David Packard Electrical Engineering building.

The EE department is in the midst of a period of significant transition—with respect to faculty and research—according to Chairman Wooley. “In addition to the recent wave of administrative changes,” he explains, “we are faced with replacing nearly one-third of our department’s faculty over the next five years, which presents us with both a significant challenge and an exciting opportunity.”

The Packard building not only provides a notable improvement in the department’s teaching and research facilities, it also unites the Electrical Engineering, Computer Science, and related faculty in a consolidated physical location for the first time. “Boundaries between EE and other disciplines are becoming less and less distinct,” maintains Wooley, “Whereas traditionally EE referred to a collection of disciplines relevant to the creation of electrical and electronic systems, today it encompasses almost any area of engineering activity that depends, in some fashion, on electrical phenomena.” Chairman Wooley feels confident that the new proximity the Packard building affords will enhance collaboration among faculty and students, encouraging the kind of interdisciplinary study that is crucial to the future of electrical engineering. □



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From Bob Dutton

Uncharted Territory

Stanford's Center for Integrated Systems is pleased to add our salutations for the new millennium. As noted in our last issue, we have witnessed many exciting changes during the close of last year—a new Provost, Dean, and EE Department Chairman, to name only three. We are now in the process of selecting a new President as well. These leadership changes reflect both the dynamic nature of Stanford and the importance placed on leadership in driving our vision towards the future.

At last fall's Advisory Committee Meeting (AdCom), we challenged our corporate sponsors with a preview of Stanford's future, in part driven by the new initiative into the broad intersection (i.e. "X-ing") of the Biological Sciences, with the university generally and School of Engineering very specifically. I would like to comment on several aspects of this Bio-X dialog, both to soften the potential fear about CIS's future in traditional microelectronics and also to give the broadest positive spin to the changes that are driving academia.

First, the good news about ongoing scaling and plentiful harvests of electronics based on "end of the roadmap" MOS technology as we now know it. At the 1999 IEDM lunch speech given by **Dr. Bob Dennard (IBM)**, there was one quote that stood out for me as capturing the essence of where silicon technology now stands:

"[It] has reached a very high plateau, not easily challenged or replaced."

This helps to quantify the most basic point. The integral under the curve of total transistor numbers and, more importantly, new higher levels of functional integration, will continue to yield even more amazing integrated electronics solutions for generations to come. The number of CIS-affiliated faculty with interest in electronics, far from dwindling, is growing; and the interest and excitement about emerging applications is becoming increasingly diverse.



The presentation by **Olav Solgaard** at the last AdCom is one example of the intersection between MEMS electronics, circuits, and optoelectronic devices (not to mention new applications). As head of one of the most recent EE Department faculty searches in the area of interface electronics, I can also reinforce the message that innovations in electronics, coupled with the need for both research and educational training in these areas, are strategic, long-term agenda items. Quoting from our search advertisement, the area we are targeting for new growth is:

"...the design of circuits employing novel and emerging mainstream semiconductor technologies to solve electronic system interface problems, with an emphasis on mixed signals (analog and digital) across diverse frequency spectra and possibly involving heterogeneous technologies in areas such as sensors, optoelectronics and bioelectronics."

In short, the intrinsic need for (and strategic leverage provided by) circuit design is in every sense alive and well. The challenges of signal acquisition and functional integration across interfaces will continue to be essential fare and a potent training ground for electrical engineers for the indefinite future.

Having stated this very positive (and obvious?!) news that circuits and functional integration using IC's will continue, there are additional points that need to modulate the vision of the future. Despite the amazing progress in creating "computational plenty" (witnessed by the PC and other hand-held devices that surpass mainframe computers of the 1970s), the human interfaces of keyboards, screens, and pointing devices have moved incrementally much more slowly. While there have been some recent shifts with new hand-held devices (personal organizers and communications systems), the basic bandwidth and range of expressiveness between humans and electronics can be starkly contrasted by two reference points:

- 1) The changes in Internet bandwidth over the past two decades.

2) The potency of all forms of digital signal processing (DSP) related to both audio and video information.

In order to put the Bio-X dynamics and academic fervor in perspective, it's useful to think about the state of knowledge at the turn of the last century and try to imagine the industrial perspective from that vantage point. Having read the

I'm sure that at the turn of the last century, there was serious discussion and doubt about the relevance of that quantum revolution. After all, the industrial revolution was still in full swing; even commercial air travel would have been considered laughable at the time. The practical realization of quantum effects with optoelectronic lasers and light-emitting devices, along with their ubiquitous use for everything, from

“...it's useful to think about the state of knowledge at the turn of the last century and try to imagine the industrial perspective from that vantage point.”

book “Crystal Fire—The Birth of the Information Age” by Michael Riordan and Lillian Hoddeson (published by Norton & Company, 1997) in celebration of the 50th anniversary of the transistor invention, I was impressed with the rapid evolution of technology events that followed the quantum mechanics (QM) revolution (which set the stage for solid state physics as we know it today). Current events in the biosciences, along with exciting new atomic scale sciences, now make coupled experimental and computational modeling possible. This is likely to change the face of both today's medicine and what we think of as “human engineering of products.” Basically, the stage is set for Bio-X style QM paradigm shifts and the resulting engineering breakthroughs. It is in the context of this landscape and intellectual environment that Stanford has launched its bold Bio-X program.

traffic lights to CD players and internet communications, would have seemed as strange as Jules Verne's vision from “20,000 Leagues Under the Sea.” In short, our ability to extrapolate where knowledge and technology will go in the future is flawed at best, and self-serving at worst.

The bottom line for this discussion is pretty simple. The Bio-X program is now formally launched at Stanford, with the truly amazing endowment from **Jim Clark**. The new James Clark facility is expected to be built directly across the street from our Paul G. Allen Center for Integrated Systems. Only the bounds of our imagination, resourcefulness, and creativity will limit where such new research opportunities will take us in the future. We look forward to exploring those opportunities productively in collaboration with our CIS industrial partners and sister academic institutions. □

CIS Notes

JOHN HENNESSY

Provost John Hennessy is the co-recipient of the 2000 IEEE John Von Neumann Medal. This medal is awarded by the IEEE for outstanding achievements in computer-related science and technology.

MARK HOROWITZ & ABBAS EL GAMAL

Professors Mark Horowitz and Abbas El Gamal have been elected Fellows of the IEEE, one of the Institute's most prestigious honors.

MARTIN HELLMAN

Professor Emeritus Martin Hellman is a co-recipient of the 1999 IEEE Koji Kobayashi Computers and Communications Award.

WILLIAM DALLY

Professor William Dally has been appointed the William George Hoover Faculty Scholar in Electrical Engineering. The appointment's duration is 9/1/99 to 8/31/2000.

HOWARD ZEBKER

Associate Professor Howard Zebker has been appointed the Robert N. Noyce Faculty Scholar Chair in the School of Engineering. The duration will be 9/1/99 to 8/31/99.

JOHN BRAVMAN

Professor John Bravman has been appointed the Bing Centennial Professor and Vice Provost for Undergraduate Education. The duration will be 9/1/99 to 8/31/2004. □

CIS World Travelers

In the acronym-laden environment of CIS, we sometimes don't completely understand what lies behind the jumble of letters that represent various programs, institutions or groups. An example of this is the SPIE program; its name may be familiar, but its purpose perhaps less so. (And because it is pronounced "spy," its mention is sometimes met with both humor and guarded acceptance.)



The SPIE team at Hitachi Central Research Lab's beautiful gardens. (Left to right: Professor Bob Dutton, Dr. Isao Yoshida, Xin Yi Zhang, and Choshu Ito.)

Since its inception in 1986, the CIS Student-Partner Information Exchange (SPIE) Program has sent over 20 teams of advanced CIS-affiliated PhD students to over 15 different partner company sites. SPIE visits allow students to give technical presentations in a professional setting, tour partner company facilities, and discuss research with industrial engineers.

Partner companies and CIS work together to identify students whose research is most relevant, and CIS's Programs and Administration Manager, **Carmen Mirafior**, then schedules a visit to the company site. "This has been a win-win-win collaboration for host companies, faculty, and students," says Mirafior, "Students come away far more prepared to give technical presentations, and they gain a broader perspective on their research from their industry colleagues. For our partners, the sneak preview of current academic research provides a strong return on investment, and an edge non-CIS companies don't have."

The visits give students an opportunity to learn more about corporate cultures, while receiving valuable feedback from industrial professionals. The exchange also keeps CIS partner companies apprised of the latest work conducted by Stanford students and serves as a leveraging tool for recruitment. CIS coordinates and covers the costs of transportation, such as airfare and car rental, while the partner company host typically

covers the expense of hotels and meals. The two most recent SPIE trips, to **Hitachi's** Japan offices in September and Germany's **Infineon** in September/October, drew rave reviews from both sides of the Atlantic and Pacific.

SPIE TRIP TO HITACHI

On Sept. 9th, a SPIE team comprised of **Professor Robert Dutton** and students **Xin Yi Zhang**, **Choshu Ito** and **Jaejune Jang** visited Hitachi's Device Development Center (DDC) in Ome,

Japan, where they were hosted by **Drs. Hiroo Masuda** and **Hisako Sato**. After a detailed overview of the ongoing projects inside the device development group, the students presented their research. Xin Yi presented "A Quasi-Mixed-Mode MOSFET Model for the Simulation and Prediction of Substrate Resistance Under ESD Stress and Layout Variations," Jaejune discussed "Circuit Model for Power LDMOS Including Quasi-Saturation," and Choshu presented "Gate Width Dependence of RF LDMOS."

The following day, the group toured the Hitachi Central Research Lab (HCRL) in the city of Kokubunji, where their gracious host, **Dr. Isao Yoshida**, also showed them around the beautiful gardens that surround Hitachi's offices. Engineers in Dr. Yoshida's group gave presentations about specific current projects and also discussed the research CIS students had presented the previous afternoon. The SPIE group was also able to tour Hitachi's RF lab.

"We were very pleased to host the recent SPIE visit," commented Dr. Hiroo Masuda, Sr. Engineer in the Process Development Dept. of Hitachi's DDC. "It provided an opportunity for updates on VLSI R&D at CIS, as well as a technological exchange and a lively discussion on culture during dinner. Our only regret was that the day could not be longer, and we hope this visit will be one of many, enhancing technical exchange and collaboration between Stanford and Hitachi."

IN THEIR OWN WORDS

"The visit to DDC allowed me to meet more Hitachi people outside HCRL. The HCRL presentations were familiar territory for me and were very interesting. I had some valuable post-SPIE visit discussions, and the people we met were very warm. I was impressed with the effort they put into making our visit so rewarding."

—Choshu Ito

(Visiting Student at HCRL)

"This was an enriching and valuable experience for me. By interacting with all the engineers, I learned more about Hitachi and their corporate culture. The technical discussions were beneficial for both the students and the Hitachi engineers. The comments and questions helped me to focus and clarify my presentation, and the feedback generated more research topics for me."

—Xin Yi Zhang

SPIE TRIP TO INFINEON

Two years ago, a SPIE team was dispatched to partner company **Siemens**, in Munich, Germany. As the *CIS Newsletter* reported, the group had an exceptionally good time (the trip suspiciously coincided with the celebration of Octoberfest),



Professor Tom Lee (second from right) with his Infineon hosts and SPIE team.

in addition to having a very productive exchange. CIS was eager to repeat the event and the opportunity presented itself when, on April 1, 1999, **Infineon Technologies**, spun-off from Siemens Semiconductors and CIS decided to obtain a glimpse of its "new" partner company.

The SPIE trip to Infineon was split into two sections. On September 24th, **Dwight** and **Rachelle Thompson** arrived at Infineon as the first wave of the CIS "invasion" (once again, suspiciously coinciding with the observance of Octoberfest). Two weeks later, the second team arrived, comprised of **Evelina Yeung**, **Gu-Yeon Wei**, and **Professor Tom Lee**.

Despite the temptations of Octoberfest, the trip wasn't all libations and lederhosen. Soon after their arrival, Professor Lee's SPIE team met with **Dr. Herbert Eichfeld** and discussed PhD research at CIS with him and his group. After a detailed introduction to the company, the SPIEs toured the research labs, where they discussed the mixed-signal projects being conducted at Infineon (in areas including RF, datacom and high-speed I/O). The SPIE team presented their research and had many opportunities to obtain feedback from Infineon scientists in both professional and social settings.

"Dwight's talk on pipelined floating-point ADC was interesting for our ADC experts, as they could learn about an architecture they don't work on," commented Dr. Herbert Eichfeld, who presided over both visits. "The presentations of Tom, Evelina and Gu on wireless/wired transceivers and low-power logic techniques were attended by many of my colleagues, and we had detailed discussions with them on these topics afterwards. My impression was that these SPIE trips were very useful to Infineon. I am looking forward to intensifying our cooperation with CIS."

IN THEIR OWN WORDS

"My SPIE trip to Infineon in Munich was a memorable experience on many levels. I was able to present current

HITACHI-JAPAN TRIP — COMMENTS FROM PROF. BOB DUTTON

This was a very exciting landmark event from several perspectives. It was our first visit to an Asian partner, and for most of the students, their first trip to Japan. **Drs. Hisako Sato** and **Hiroo Masuda** were excellent hosts at the DDC, giving us a nice overview of DDC's broad set of product activities.

Two specific and exciting events at DDC included:

- A detailed discussion with **Dr. Atsushi Hiraiwa** about our newest results on quantum inversion layer charge and tunneling current effects on capacitance extraction.
- Meeting **Mr. Akio Shima**, a possible visiting scientist candidate in the area of shallow junction technology.

Dr. Isao Yoshida hosted our second-day visit to the CRL and again we had exciting discussions with several researchers interested in modeling limits for scaled analog and especially RF devices. **Dr. Shiro Kamohara**, an expert in BSIM models and former visitor at UC Berkeley with Prof. **Chenming Hu**, was especially interested in exciting opportunities to use advanced device analysis (TCAD tools from Stanford) to improve circuit model accuracy.

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From Richard Dasher

On the Value Leveraged by CIS Membership

CIS provides value to our Partner Companies by opening “windows” to the full range of Stanford activities and people in areas of interest to our Partners, as well as by funding Stanford faculty research and FMA PhD fellowships in our areas of focus. In our most recent AdCom meeting (11/99), the CIS Industry Advisory Committee asked us to investigate the value of these broader associations leveraged by CIS membership.

The total research volume of Stanford’s School of Engineering (SOE) for the 1997-98 accounting year was \$85.5 million.¹ Of course, this amount includes some areas only peripherally relevant to CIS, but CIS stands at the nexus of many of the School’s domains of research strength. Through CIS, Partner Companies have provided support to over 50 Stanford faculty, which corresponds to about 23% of all Stanford engineering professors. One rough calculation of the value of CIS-affiliated faculty research (as a simple percentage of the SOE total) would thus be \$19.7 million, almost ten times greater than the CIS research budget.

Moreover, the value of CIS-relevant research is probably higher, because CIS-affiliated faculty are productive. Our investigation has revealed that CIS-affiliated professors supervise over 475 PhD students at the present time, an average of 9.33 PhD students each. This represents a greater than 20:1 ratio between (a) the total number of Stanford PhD students in areas of interest to CIS companies and (b) FMA PhD fellows that receive support through CIS.

This pool of PhD students probably comprises about 40% of all currently enrolled engineering PhD students at Stanford.² If one applies that ratio to pre-Masters and PhD candidates, about 1,130 of the 2,842 SOE graduate students registered in 1998-99 have technical interests relevant to our Partner Companies.



CIS assists Partner Companies in arranging recruiting activities aimed at these students, including our publicizing of opportunities for summer jobs and permanent positions. Other windows that CIS opens for our Partner Companies include:

- “Student-Partner Information Exchange” (SPIE) visits by advanced PhD students to Partner Companies (see article pg. 4)
- The opportunity to send a Visiting Scientist in residence at CIS
- Technical seminars for company researchers to present and discuss their findings at Stanford
- Distribution of selected PhD oral defense

- presentations to Partner Companies (via videotape)
- Searchable databases of research projects, faculty, and students on the CIS website
- Announcements of relevant news and events at Stanford
- This newsletter

The value of CIS membership, however, depends as much on the Partner Company as on the size of Stanford’s research base. From our AdCom representatives, I often hear that there is a direct correlation between their level of involvement and the value of CIS membership. Moreover, CIS will always work closely with our Partner Companies to facilitate the involvement of additional Partner Company personnel who may benefit from the relationship. Although the time constraints on corporate researchers and R&D managers are increasingly severe, even a little involvement leverages a lot of potential value. □

¹ School of Engineering statistics are from the Stanford University School of Engineering Facts Brochure 1998-1999. This is the most recent data available at the time of writing. See also <http://soe.stanford.edu/AR97-98/index.html>.

² This percentage is based on an estimate of about 1,200 PhD students in SOE at any one time. We calculated this estimate by multiplying the 266 PhD and Engineering degrees awarded in 1997-98 by 4.5, the average number of years required to obtain a PhD.

MEMBER FEE INCREASE

Per discussion in our 11/99 meeting with the Industry Advisory Committee, CIS will increase its membership fees. The new yearly fees will be:

- Full Partner: \$150,000
- Associate Partner: \$75,000

This increase, the first in the fifteen-year history of CIS, will be reflected on all invoices sent out after January 1, 2001. Since we invoice most of our Partner Companies in the summer, the new fee

schedule will affect most members from autumn 2001.

This increase is needed to offset increased costs of supporting student fellowships and research customization projects. The cost of a graduate student research assistant has risen well above the \$30,000/year that CIS currently provides to faculty for an FMA. Since some Partner Companies implement their research customization project as a second FMA, we are increasing the allocation for this category as well. The new

standard yearly allocations will be \$45,000 for each FMA and research customization project. As in the past, Partner Companies can support additional FMAs or custom projects at cost.

These new allocations will take effect from the time a company first pays the new, higher fee. Therefore, in most cases, faculty will see the new FMA and research customization amounts beginning in autumn 2001. □

Alumni Spotlight - Dr. Alvin Loke

The Alumni Spotlight is a series of articles that catches up with former CIS students for an update on their current work. In this issue, Dr. Alvin Loke of **Agilent Technologies/CSP** talks to the *CIS Newsletter* from his new post in Singapore.

Ever since my early childhood, I've been naturally inquisitive about science and engineering. My father, a mechanical engineer himself, was instrumental in developing my interests in math and science.

After graduating from Stanford, I chose to work at **Hewlett Packard** (HP). I had heard many positive things about HP Labs and knew it was a good starting place, where I could be creative and learn a lot in a friendly culture. During my stay at CIS, I became well acquainted with my hiring managers, **Paul Rissman** and **Gary Ray**, before joining the ULSI Research Lab.

Since the **Agilent Technologies** spin-off from HP, I've been concentrating on copper interconnect technology as an assignee to **Chartered Silicon Partners** (CSP), Agilent's IC manufacturing arm in Singapore. I'm currently working on process integration of on-chip IC interconnects. At HP Labs, I was involved in the integration of nonvolatile ferroelectric random access memory (FeRAM). HP had a joint venture with **Texas Instruments** to demonstrate the feasibility of incorporating FeRAM into a 0.18- μm process technology. We successfully fabricated the smallest integrated ferroelectric capacitors reported to date.

My project on FeRAM technology has the potential to replace embedded Flash, embedded DRAM, and non-cache SRAM memories, and could be a key enabler for future system-on-a-chip applications. The manufacturability of this technology remains to be demonstrated, but the demand for embedded memory technology will only increase with the incessant thirst for higher performance IC's.

My new project at CSP will be to ramp-up copper technology into manufacturing. Copper interconnects enable chips to miniaturize even further, for higher performance. This new role is not research-oriented. However, it's been very exciting bringing a cutting-edge technology to maturity, especially since I worked on copper technology for my thesis. It's also a great opportunity to work in an Asian foundry.

The biggest challenge I've faced so far is learning to be flexible. Technical directions in the industry are driven by business opportunities and a rapidly changing market climate. Change is difficult to deal with at times, but it's an important reality in the high-tech workplace. Support from peers and management certainly helps a lot.

It's becoming increasingly obvious that finding time for continuing education will not be easy. This makes it even more important to learn from peers and stay in touch with friends. One of the benefits of CIS is that you make friends with fellow

engineers who have developed expertise in a wide range of technical fields. One can gauge the activities and trends that are important in the industry by staying in touch. I think industry is doing an adequate job of training engineers, but CIS plays a large role in making this training process a relatively smooth one.



Dr. Alvin Loke

I had a wonderful time at CIS! Although much hard work and many long hours were involved, I met lots of good friends, interacted with many brilliant people, and learned a myriad of amazing things in a friendly atmosphere. Personally, it was a very nurturing environment to learn in while away from home. Without a doubt, CIS had a very positive impact on my education.

I really enjoyed working with my advisor, **Professor Simon Wong**. He strongly emphasized our CIS education as training to work in industry, and fostered a tight group atmosphere and teamwork spirit among his students. He also encouraged extensive interaction with industry (to glean a good understanding of how things are done outside the university and establish connections). I made some close friends in Professor Wong's group, and continue to stay in touch with them.

I participated in a few SPIE trips, the FMA program, and poster board sessions during CIS's AdCom meetings. These interactions were wonderful opportunities to expose my work and gain valuable feedback from industry experts on which aspects of my research were pertinent and which were esoteric.

My advice to CIS students is learn to be flexible! The only constant in the high-technology industry is change—accept it as a fact of life and learn from it. Also, find a good mentor. While at CIS, I was extremely fortunate and grateful to develop a great working relationship with **Jeff Wetzel** of Motorola, who later became my co-advisor. When I joined HP, I was very lucky to have **Shawming Ma**, another CIS graduate, continue this mentoring role. Lastly, although it may seem difficult at times, enjoy yourself at CIS! It's a great time to learn a lot, meet interesting people, make great friends, and have fun. □

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research that I've been working on at Stanford and get lots of good feedback and an understanding of the issues that engineers in industry are concerned with. Many times, industry's approach differs from academia's. In addition, we got a tour of the labs there, a look at the projects they're working on, and a glimpse of the cutting-edge products that we can anticipate in the near future. On a completely different note, the experience of going to Germany for a couple of days was wonderful. I had never considered looking outside of Silicon Valley for a job, but now... who knows? Maybe I could end up somewhere in Europe. The prospect is exciting." —**Gu-Yeon Wei**

"I presented a talk on a 15-bit Pipelined Floating-Point A/D Converter. During my visit to Infineon, I learned of the numerous products designed by my hosts. My visit also occurred during Oktoberfest, so I was able to see the "Big Tents" at the festival, and take in a quick tour of Munich."

—**Dwight Thompson**

INFINEON-GERMANY TRIP — COMMENTS FROM PROF. TOM LEE

The SPIE trip was great—my first day there overlapped with the last day of Oktoberfest, so I got to take subway rides with nearly comatose revelers from all over the world!

The visit to Infineon was simply terrific. The first full day began with a discussion of **Ulrich Barnhoefer's** research. (Ulrich recently changed his status from Infineon'er to full-time Stanford PhD student.) All were enthusiastic that his work represented a promising new approach to low-power transceiver design. Ever the perfect host, **Herbert Eichfeld** arranged a tour of the facilities, where we had the opportunity to speak with researchers from a number of different groups within Infineon. Gu, Evelina and I were all very impressed with the high quality of the research and with the wonderful discussions we had with Infineon's engineers. On the second day, the three of us presented talks on Stanford research. These were well attended, and I was particularly amazed at the detailed notes taken by at least one Infineon researcher. In post-presentation discussions, he had many deep, insightful questions that proved he wasn't just doodling on the notepad. In fact, it appeared that he had virtually transcribed our talks! The students and I benefited greatly from having Infineon researchers ask such detailed questions (and, in more than one case, raising issues no one else ever had). This only deepened an already close relationship between my group and Infineon.

I would call this a highly successful SPIE visit, and I look forward to the next one. I know that the students feel the same way, because they said so!

"The trip was very rewarding for me. First of all, it was very helpful learning more about Infineon. Moreover, the information exchange allowed both sides to obtain valuable feedback on their work. The questions, during both the presentation and the discussion session afterwards, gave me hints as to which

parts of my presentation were unclear and how I could improve them, and also guided me toward other interesting research questions. It was also very helpful for me to learn more about Infineon's ongoing work in high-speed I/O design, which is my area of research." —**Evelina Yeung** □

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