A 1.8-V Digital-Audio Sigma-Delta Modulator in 0.8-μm CMOS*

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Abstract — **Oversampling techniques based on sigma-delta (ΣΔ) modulation offer numerous advantages for the realization of high-resolution analog-to-digital (A/D) converters in a low-voltage environment. This paper examines the design and implementation of a CMOS ΣΔ modulator for digital-audio A/D conversion that operates from a single 1.8-V power supply. A cascaded modulator that maintains a large full-scale input range while avoiding signal clipping at internal nodes is introduced. The experimental modulator has been designed with fully-differential switched-capacitor integrators employing different input and output common-mode levels and boosted clock drivers in order to facilitate low voltage operation. Precise control of common-mode levels, high power supply noise rejection, and low power dissipation are obtained through the use of two-stage, class A/AB operational amplifiers. At a sampling rate of 4 MHz and an oversampling ratio of 80, an implementation of the modulator in a 0.8-μm CMOS technology with metal-to-polycide capacitors and NMOS and PMOS threshold voltages of +0.65-V and –0.75-V, respectively, achieves a dynamic range of 99 dB at a Nyquist conversion rate of 50 kHz. The modulator can operate from supply voltages ranging from 1.5 V to 2.5 V, occupies an active area of 1.5 mm^2, and dissipates 2.5 mW from a 1.8-V supply.**

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I. INTRODUCTION

Rapid growth in the demand for portable, battery operated electronics for communications, computing and consumer applications, as well as the continued scaling of VLSI technology, has begun to significantly alter the constraints under which many semiconductor integrated circuits are designed. In particular, in order to both conserve power in digital circuits and reduce the high electric fields that accompany the scaling of device dimensions, it is becoming necessary for circuits to operate from reduced supply voltages. Without the use of voltage regulation, the minimum supply voltage in portable equipment is generally the end-of-life battery voltage multiplied by the number of cells connected in series. In the case of nickel-cadmium and alkaline cells, the end-of-life voltage is 0.9 V, corresponding to a 1.8-V minimum supply voltage for two batteries in series.

Considerations such as cost, performance and portability are powerful incentives for integrating analog and mixed-signal circuit functions, such as data conversion, on the same chip as large digital data and signal processing circuits. However, even supply voltages as large as 5 V severely constrain the dynamic range available for realizing analog circuits with the performance that is increasingly demanded in communications and multimedia applications. Thus, it is an

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especially challenging task to maintain the desired levels of performance as the supply voltage is lowered. Moreover, while a reduction in supply voltage generally results in significant power savings in digital circuits, the power consumed in analog circuits is actually likely to increase.

Among the most critical, and often performance limiting, functions in mixed-signal VLSI circuits are the interfaces between analog and digital representations of information. As a consequence, considerable attention is being given to the design of CMOS analog-to-digital converters that operate from supply voltages below 5 V with reduced power dissipation. Much of the work reported to date focuses on the realization of low-power, low-voltage oversampling converters for voiceband telephone applications [1]-[5] and the use of pipelining and folding to implement power-efficient video-rate converters [6]-[9]. In the case of oversampling converters, alternative CMOS circuit approaches, such as switched-capacitor, switched-current and continuous-time circuits, have been explored. This work presents the results of research into the design of oversampling sigma-delta modulators that provide the performance required for high-fidelity, digital-audio applications when operated from supply voltages as low as 1.5 V and dissipating only a few mW of power [10].

Sigma-delta modulation is a robust means of implementing high-resolution analog-to-digital converters in a VLSI technology. By combining oversampling and feedback to shape the noise, and then using a digital lowpass filter to attenuate the noise that has been pushed out-of-band, it is possible to achieve a dynamic range as high as 16 bits or more at relatively modest oversampling ratios [11]. Moreover, as shown herein, oversampling architectures are potentially a power-efficient means of implementing high-resolution A/D converters. In effect, an increase in sampling rate can be used to reduce the number and complexity of the analog circuits required in comparison with Nyquist-rate architectures, transferring much of the signal processing into the digital domain where power consumption can be dramatically reduced simply by scaling the technology and reducing the supply voltage.

This paper describes what is believed to be the first reported high-fidelity, digital-audio sigma-delta modulator that operates from a power supply of only 1.8 V and dissipates less than 3 mW of power. It is shown that the overall power consumption of a sigma-delta modulator can approach that of a single integrator with the resolution and bandwidth required for a specific application. Furthermore, the continued scaling of CMOS technology has made low-power implementation of the accompanying decimation filter practical, and power dissipation comparable to that achieved for the modulator can be expected for the digital filter [12]. The relaxed requirements for the analog antialiasing filter in an oversampled A/D converter also represent a significant power dissipation advantage in comparison with Nyquist rate converters.

The experimental modulator described herein employs switched-capacitor circuits and has been integrated in a 0.8-µm CMOS technology with NMOS and PMOS threshold voltages of

+0.65-V and –0.75-V, respectively. It provides a dynamic range of 99 dB and a peak SNDR of 95 dB for a signal bandwidth of 25 kHz. It operates from a 1.8-V supply and dissipates 2.5 mW.

The fundamental limits on power dissipation in switched-capacitor sigma-delta modulators are explored in Section II. The impact of low-voltage operation is evaluated, and strategies to overcome the problems it presents are identified. Section III describes the design of an experimental modulator that provides digital-audio performance when operated from a 1.8-V supply. The measured data for the experimental modulator and the operational amplifier used in its implementation are presented in Section IV.

II. Fundamental Limits

Fig. 1 is a simplified diagram of a single-stage, one-bit sigma-delta modulator comprising a switched-capacitor integrator followed by possible additional discrete-time filtering, represented by $A(z)$, and a one-bit quantizer. Gain in the forward path of the feedback loop desensitizes the modulator's output to subsequent disturbances and component nonidealities along the forward path. Errors within the low-frequency signal baseband are attenuated, while those at higher frequencies are amplified. This phenomenon, known as noise shaping, applies to circuit imperfections as well as the quantization error introduced by the quantizer. The order of shaping to which a particular error in the forward path is subjected is equal to the order of filtering preceding the point in the circuit at which the error is introduced. Errors introduced at the input node are simply added to the signal and thus degrade the overall modulator performance directly.

Owing to the noise shaping, among the circuits in the forward path of the sigma-delta modulator in Fig. 1 the first integrator stage has by far the greatest influence on the modulator's performance. Nonidealities such as kT/C noise, amplifier noise, incomplete settling, and harmonic distortion in this circuit must generally meet the overall performance requirements specified for the A/D converter. Errors in the subsequent filter and quantizer can be much greater than those introduced in the first stage without significantly impairing the modulator's performance.

The power consumed in a switched-capacitor integrator is generally proportional to its loading. Therefore, to minimize the power dissipation when such an integrator is used as the first stage of a sigma-delta modulator, the smallest capacitor sizes for which the required converter resolution and bandwidth can be maintained should be used. This approach leads to a modulator design for which the performance is limited primarily by kT/C noise in the first integrator. For this reason, the remainder of this section is devoted to considering the design of low-power, switched-capacitor integrator stages capable of operating from low supply voltages. First, the estimates of theoretical minimum power dissipation in switched-capacitor first-stage integrators implemented using ideal class A and class B amplifiers is established. The impact of practical implementation issues is then considered. Finally, a number of amplifier circuits are introduced, and their performance is evaluated in the context of low-voltage, low-power integrator design.

A. Ideal Switched-Capacitor Integrator Power Dissipation

Fig. 2 illustrates a fully differential switched-capacitor integrator suitable for use as the first stage of the modulator in Fig. 1 and implemented using an ideal operational amplifier. In the following equations, it is assumed that the amplifier has infinite bandwidth and gain, that its output can swing from rail-to-rail, that there are no parasitic capacitances, and that the only noise in the integrator is that due to the sampling switches. The noise power within the baseband of an oversampling modulator introduced by a first stage integrator of the form shown in Fig. 2 is then

$$S_{kT/C} = \frac{4kT}{MC_S} \quad , \tag{1}$$

where k is Boltzmann's constant, T is the absolute temperature and M is the oversampling ratio and is equal to the modulator sampling rate, f_S, divided by the Nyquist sampling rate, f_N. The factor of 4 accounts for the two paths through which noise is sampled (during $\Phi 1$ and $\Phi 2$) and the fully differential structure of the circuit.

If the maximum amplitude of the differential input to the modulator is V_{sw}, then the power of a full-scale sinusoidal input is

$$S_S = \frac{V_{sw}^2}{2} \quad . \tag{2}$$

The dynamic range (*DR*) of the modulator is defined as the ratio of the power in a full-scale input to the power of a sinusoidal input for which the signal-to-noise ratio is one (0 dB). Thus, for a modulator whose baseband noise is dominated by *kT/C* noise in the first integrator stage, the dynamic range is

$$DR = \frac{S_S}{S_{kT/C}} = \frac{V_{sw}^2 MC_S}{8kT} \quad . \tag{3}$$

As the analysis presented in the Appendix indicates, when implemented with an ideal class A amplifier, the minimum power dissipation in the first integrator stage can be estimated as

$$P = 32kT \times DR \times f_N \quad , \tag{4}$$

where DR is expressed as a ratio rather than in dB and f_N is the Nyquist sampling rate corresponding to the signal baseband. When implemented with an ideal class B amplifier, the power dissipation is

$$P = 4kT \times DR \times f_N \times \frac{\overline{\Delta V_{in}}}{V_{DD}} \quad , \tag{5}$$

where $\overline{\Delta V_{in}}$ is the average difference between the sampled differential input and feedback signals, V_{in}-V_{ref}, and V_{DD} is the supply voltage.

Equations (4) and (5) indicate that the minimum power dissipation in the first stage of an oversampling modulator depends linearly on the required dynamic range, DR. Since for every additional bit of resolution the DR must be increased by a factor of 4 (6 dB), the power dissipation depends strongly on the resolution. The dependence on the Nyquist conversion rate, or equivalently the signal bandwidth, is linear. A key characteristic of the analytical results expressed in (4) and (5) is the absence of the oversampling ratio and, in the case of the class A amplifier, the supply voltage. Thus, the dependence of power dissipation on these factors is primarily an implementation issue.

The power consumed by most practical oversampling A/D converters is typically three or more orders of magnitude greater than that predicted by the fundamental limits represented by (4) and (5). This is a consequence of the impact of various nonidealities, some of which are considered in the following subsection.

B. Impact of Circuit Nonidealities on Integrator Power Dissipation

Equations (4) and (5) assume the use of ideal operational amplifiers and, thus, ignore the bandwidth and settling time of the integrator. Settling is one of the important factors increasing the power dissipation significantly above the levels predicted by (4) and (5). In response to a step input, the integrator output typically slews for some time and then enters a linear settling regime. In high resolution applications, linear settling is usually needed to achieve the full resolution of the converter. Therefore, in practice, the integrator settling time is substantially greater than it would be if the integrators were only slew limited. Consequently, the power dissipation for a given f_N is increased relative to that predicted by (4) and (5).

In many operational amplifier circuits, the settling time constant is a function of the size of the input transistors. While the transconductance of the input devices increases as the square root of the input transistor aspect ratio, the amplifier load also increases with the size of the input transistors. For an integrator of the form shown in Fig. 2, the effective amplifier load is equal to the integration capacitor in series with the parallel combination of the sampling capacitor and the amplifier input capacitance. Thus, the input transistor size that minimizes the integrator settling time constant depends on the sampling capacitor size and, hence, on the *DR*.

If the oversampling ratio and f_N of a modulator are held constant and its dynamic range is increased, the size of the sampling capacitors in the first stage must also be increased. This allows for the use of larger input transistors, which thereby reduces the fraction of the settling time due to linear settling. Thus, the power dissipation in the modulator moves closer to its fundamental limit as the resolution is increased. On the other hand, if the oversampling ratio and dynamic range of a modulator are held constant while f_N is increased, the settling time must be decreased proportionally to maintain the required settling precision. If the first-stage integrator is implemented with a class A amplifier, then although slew rate increases linearly with tail current the settling time constant only decreases in proportion to the square root of the tail current. Therefore, the fraction of the settling time due to linear settling becomes larger as the tail current is increased, and the power dissipation of the converter increases relative to the level predicted by the fundamental limit. Thus, for a class A amplifier, the power dissipation transitions from a linear to a quadratic dependence on f_N instead of following the simple linear dependence predicted by (4) and (5).

Another important practical deviation from the ideal equations is the limited amplifier output swing. To maintain a constant *DR* as supply voltage is scaled down, the noise power must be reduced by the same amount that signal power is reduced. This implies that capacitor sizes, and hence amplifier currents, be increased by the same proportion that signal power is reduced. Since signal swing scales proportionally faster than supply voltage, there is a net increase in power dissipation as supply voltage is reduced, as is apparent in equations (18) and (22) in the Appendix.

While equations (4) and (5) take into account only *kT/C* noise arising from the sampling network, the amplifier also contributes noise within the baseband. The two dominant types of amplifier noise in digital-audio applications are 1/*f* noise and broadband thermal noise. Several circuit techniques are commonly used to suppress 1/*f* noise: chopper stabilization, correlated double sampling, and transistor sizing. However, broadband noise cannot be greatly reduced in a power efficient manner. Typically, the best noise performance is obtained with a simple differential-pair input stage since folded structures introduce additional noise sources. When the amplifier thermal noise is dominated by the noise of a differential-pair with current source loads, the input-referred thermal noise of the first integrator integrated over the bandwidth of the amplifier is

$$S_{N,\,amp} = \frac{2kT}{MC_C} \times \frac{\gamma}{1 + C_S / C_I} \times \left(1 + \frac{g_{m3}}{g_{m1}}\right), \qquad (6)$$

where C_C is the amplifier compensation capacitor, γ is the noise enhancement factor of short channel transistors [13], g_{m1} is the transconductance of the input transistor and g_{m3} is the transconductance of the load transistor. Increasing the compensation capacitor reduces the amplifier thermal noise but requires higher currents to obtain the desired bandwidth. A reasonable compromise is achieved by choosing C_C equal to C_S so that the amplifier thermal noise has approximately one half the power of the sampling noise.

A significant simplification in subsection A is the omission of parasitic capacitances. As mentioned earlier, the amplifier input capacitance can limit the settling response of the integrator. Another important consideration is the bottom plate parasitic of the integration capacitor, which directly loads the amplifier output. In an integrator with a gain of 0.2, a bottom-plate parasitic equal to 20% of the nominal capacitance can increase the settling time constant by more than a factor of two. This, in turn, necessitates a commensurate increase in power dissipation to maintain the required settling time response. Reducing the integrator gain requires the use of larger integration capacitors which increases the bottom plate parasitic at the output and tends to increase power dissipation. Transistor, wiring, and switch capacitances can also have an appreciable impact on the power dissipation.

Equations (4) and (5) show no power dissipation dependence on the modulator oversampling ratio, M. The implicit assumption is that, as M is increased, the capacitor sizes can be decreased by the same proportion to maintain constant noise levels, as indicated by (1). Therefore, the settling response can be held approximately constant without an increase in power dissipation. In practice, matching considerations can limit the reduction in capacitor sizes, while the contribution of parasitic capacitances, particularly at the amplifier input, becomes more severe as the sampling capacitor size is reduced. This can, in turn, limit the extent to which the size of the input transistors can be scaled, thus requiring higher currents to maintain the settling response.

The idealized amplifiers assumed in subsection A have no ancillary current paths. In practice, amplifier structures require additional circuitry and current for biasing and common-mode feedback. It is therefore important to use circuits for these functions that consume as little current as possible, employing techniques such as switched-capacitor common-mode feedback so as to avoid the use of additional differential-pairs.

Additional practical considerations are the degradation in settling time that can result from the feedforward zero of the switched-capacitor integrator during the integration phase, as well as noise coupling through the supplies, substrate and bias lines that can increase the baseband noise floor and introduce harmonic distortion.

C. Comparison of Amplifier Topologies

The choice of amplifier topology plays a critical role in low voltage, low power integrator design. The merits of three topologies are examined here: a folded cascode circuit, a two-stage class A amplifier, and a hybrid two-stage class A/AB design. Simplified circuit schematics for these configurations are presented in Figs. 3(a), (b), and (c), respectively. Table 1 summarizes the approximate dependence of key performance metrics on various device and circuit parameters. The folded cascode topology has the highest non-dominant pole, and thus provides the highest frequency performance. However, it also has the lowest output signal swing and is somewhat noisier than the other circuits.

The two-stage class A amplifier in Fig. 3(b) has a lower non-dominant pole than the folded cascode circuit. However, in low frequency applications the current needed in the second stage for slewing also serves to ensure a good phase margin. In high speed applications, the two-stage class A circuit requires high currents in the second stage to push out the lowest non-dominant pole, thus significantly increasing its power consumption. A shortcoming of the two-stage class A amplifier is its power supply rejection ratio (PSRR) from the bottom rail, which is particularly poor at high frequencies. The resulting common-mode signal can give rise to a differential-mode error because of device mismatch in the fully differential circuit. Biasing of the class A amplifier is typically accomplished with a common-mode feedback circuit that senses the output common-mode voltage in order to control the tail current source via a current mirror. However, owing to stability considerations the gain and bandwidth of the common-mode feedback loop are limited to at most those of the differential mode signal path.

The two-stage class A/AB amplifier of Fig. 3(c) combines a simple differential-pair as the first stage with current mirrors as the second stage. Due to the class AB operation in the second stages, slew limiting only occurs in the first stage. The second stage currents are chosen so that the non-dominant poles are sufficiently high in frequency to ensure stability. Because of the push-pull operation, the lowest non-dominant pole in the class A/AB design is governed by the time constant formed by approximately twice the transconductance of the output NMOS transistor and the load capacitance. Thus, the output branch current can be about half that used in the two-stage class A circuit for the same non-dominant pole frequency. When this fact is exploited together with the use of gain in the second-stage current mirrors, a significant reduction in power dissipation can be achieved relative to the two-stage class A topology. Increasing the gain in the current mirrors does lower the mirror pole and will eventually degrade the phase margin of the circuit. Therefore, the power dissipation advantage of this circuit is only attained in relatively low-speed applications. Even with a current mirror gain of one, however, the power dissipation of the circuit is at least comparable to that of the two-stage class A design.

A consequence of using current mirrors in the second stage of the class A/AB design is that the common-mode output voltage of the first stage influences the bias currents in the second stage but does not affect the second-stage output voltage. It is thus not possible to stabilize the common-mode voltages in the circuit with a single feedback loop. The common-mode voltages of the two stages can be established with high precision through the use of two independent common-mode feedback loops with bandwidths that can exceed the bandwidth of the differential-mode signal path. Furthermore, noise on the bottom supply rail appears as a common-mode input to the second stage and is thus attenuated by the common-mode rejection of that stage. Consequently, the PSRR of this circuit is superior to that of the two-stage class A amplifier.

The minimum power supply voltage from which the three different amplifiers can operate is governed by the input stage if the circuits are implemented in a technology wherein only transistors with conventional high threshold voltages are available. In that case, all three amplifiers have the same minimum supply level, which is equal to sum of the common-mode input level, the gate-to-source voltage of the input transistors, and the saturation voltage of the tail current source. In switched-capacitor integrators of the form shown in Fig. 2, the input and output common-mode voltages can be set independently. Therefore, by using a low input common-mode voltage of 400 mV and saturation voltages of 150 mV, integrators implemented in a technology with 800-mV device thresholds can be operated from supply voltages as low as 1.5 V. If the minimum supply voltage is governed by the output stage, as may be the case for amplifiers realized in a technology in which low threshold voltage transistors are available, the two-stage circuits can operate from lower supply levels.

Fig. 4 plots hand calculated estimates of power dissipation in the first-integrator of an oversampling modulator as a function of supply voltage. The power dissipation in all three circuits increases sharply at low supply voltages. The larger output swing of the two-stage amplifiers does make them more suitable for low voltage operation. Fig. 5 plots estimates of the power dissipation as function of oversampling ratio for all three amplifier topologies. At low oversampling ratios, the power dissipation is essentially independent of the oversampling ratio, while at high oversampling ratios the power dissipation rises rapidly with the oversampling ratio. The increase in power consumption at high oversampling ratios is due to the increased impact of parasitic capacitances as the sampling and integration capacitors are reduced in size. Based on the results presented in Fig. 5, an oversampling ratio of 80 was chosen for the experimental prototype described herein so as to ensure operation in the low-speed regime while retaining the benefits of a reasonably high oversampling ratio. A two-stage class A/AB amplifier has been adopted because of its low power dissipation, its good control of common-mode levels, and its rejection of power supply noise.

III. MODULATOR DESIGN

A. Modulator Architecture

With an oversampling ratio of 80, third-order noise shaping is needed to attenuate the quantization noise to a level acceptable for digital-audio applications. This can be achieved with either a single-stage or a cascaded architecture. Single-stage modulators of third, or higher, order suffer from potential instability [11]. To ensure the stability of such a topology, the maximum input amplitude is typically limited to a fraction of the feedback reference levels. However, in a modulator with performance that is limited by circuit noise, the dynamic range is maximized by maximizing the input signal. This dilemma becomes especially acute at low supply voltages. Therefore, a 2-1 cascaded structure [14] was adopted in order to allow for a high maximum input level.

A block diagram of the modulator is shown in Fig. 6. In this implementation, the integrator gains were chosen to provide an input overload level of –1 dB with respect to the differential feedback reference voltage, while maintaining integrator output swings well within the linear output range of the amplifiers. The input signal amplitude has been maximized by using the full supply rails as the reference voltages. By equating the input and feedback gains of the first integrator, the input and feedback sampling functions can share the same capacitors, thereby reducing the *kT/C* noise compared with designs where these gains are different. Behavioral simulation using MIDAS [15] predicts a quantization noise floor of –105 dB for the modulator of Fig. 6. For experimental purposes, the two 1-bit outputs are combined off-chip with the following error cancellation filters

$$H_1(z) = z^{-1} , \tag{7}$$

$$H_2(z) = 4(1-z^{-1})^2 . \tag{8}$$

The resulting digital signal is then digitally low-pass filtered and the sampling rate is lowered to the Nyquist rate for the input signal by a decimation filter implemented in software.

Hardware implementations of digital decimation filters are typically composed of a cascade of comb filters that decimate by the oversampling ratio divided by four and are followed by FIR or IIR filters that decimate by a factor of 4 [11]. A comb filter computes a running average of its inputs and must perform division by its decimation ratio. When the decimation ratio of the comb filter is an integer power of 2, the division can be performed with a binary shifter. In this work an oversampling ratio of 80 is used, which requires decimation by 20 in the comb filters. Division by 20 can be performed efficiently in hardware by expressing the divisor with the following sum

$$\frac{1}{20} = \sum_{k=2}^{\infty} \left(\frac{-1}{4}\right)^{k} = \frac{1}{16} - \frac{1}{64} + \frac{1}{256} - \dots \ , \tag{9}$$

using the first two or three terms, and computing the result with shifts and adds.

B. Circuits

The modulator has been designed so that its resolution is limited by thermal noise. With 4-pF sampling capacitors, using (1) as an upper bound for the *kT/C* noise of the input network, a noise floor of −105 dB relative to a rail-to-rail input sinusoid is expected due to sampling in the first integrator. With 4-pF compensation capacitors and a unity gain frequency of 24 MHz, using (6) as an estimate of the integrated amplifier thermal noise, a noise floor of −107 dB is expected due to the first amplifier. These two effects limit the noise floor of the first integrator to −103 dB. The overall noise floor includes the effect of quantization noise and thermal noise in subsequent stages, and is estimated to be −100 dB.

A key consideration in the design of the first-stage amplifier is its input-referred 1/*f* noise. The magnitude of this noise can be reduced simply by employing sufficiently large transistors in the input stage. Other options for 1/*f* noise reduction include circuit techniques such as chopper stabilization and correlated double sampling. In this work, two versions of the experimental circuit were implemented: one used correlated double sampling, while the other relied on the input transistor gate area to suppress 1/*f* noise. Experimental measurements indicate that transistor sizing alone was sufficient. In this design the input transistors are 120 μm / 1.2 μm and the load transistors are 8 μm / 2 μm.

Settling time is another important design consideration. It has been shown that sigma-delta modulators can achieve high resolution performance even if the integrators do not settle to the full resolution of the converter, as long as the settling process is linear and has no slew limited component [16]. However, to avoid slew limiting a large overdrive voltage must be used for the input transistors. This makes it impossible to use levels close to the supply rails for the feedback reference voltages, thus constraining the dynamic range of a modulator that is limited by circuit noise. Consequently, the first integrator has been designed to settle to the full resolution of the converter.

The integrators have been implemented using two-stage, class A/AB amplifiers. Shown in Fig. 7 is a schematic of the amplifier. The use of PMOS input transistors makes it possible to set the input common-mode level close to ground. This, in turn, makes it possible to use relatively small

NMOS transistors for switches that connect nodes that are at the low common-mode input voltage. The compensation network is composed of transistor M_z and capacitor C_C. M_z operates in the triode region and cancels the right half plane zero. Due to the low supply voltage, the gate of M_z was tied to an on-chip, low ripple voltage doubler.

A differential-mode half-circuit for the amplifier is shown in Fig. 8(a). The sign inversion represents the cross-coupling in the fully-differential circuit. If the current mirror is designed so that its response does not have a significant impact at the frequencies of interest, and if the transconductances of M_5 and M_7 are equal, then the half-circuit simplifies to that shown in Fig. 8(b). With this simplification it is apparent that the circuit is simply a two-stage amplifier with the second stage operating in push-pull fashion. The quiescent currents in the second stage are controlled by the output common-mode voltage of the first stage.

The common-mode half-circuit of the amplifier is illustrated in Fig. 9. It is evident that the common-mode output voltage of the first stage is coupled to the common-mode output of the second stage only through C_C. Therefore, two independent feedback circuits are needed to establish the common-mode voltages at the outputs of the first and second stages. The common-mode output of the first stage is set to the voltage that establishes the desired quiescent currents in the second stage, while the common-mode output of the second stage is set to midsupply. Two-stage designs employing a single common-mode feedback loop require a sign inversion in the common-mode feedback loop that is commonly obtained with a current mirror. To avoid compromising the stability of the common-mode feedback path, the current mirror usually dissipates a significant amount of power. In the two-stage class A/AB amplifier the two common-mode feedback loops each include only a single stage of gain, and the power dissipation of the current mirror is avoided; the two common-mode feedback loops actually consume less current than the single loop in a two-stage class A design.

The first stage common-mode feedback circuit is shown in Fig. 10. V_{cs} is the quiescent bias voltage for the tail current source. V_{cmo} is the common-mode output voltage of the first stage, which is set by a replica bias circuit so as to establish the desired quiescent currents in the second stage. The gain and bandwidth of the first stage common-mode feedback loop are greater than those of the first stage of the differential mode signal path due to the higher current and higher aspect ratio of M_{13} than the input transistors, the cascoding effect of the input transistors, and the absence of Miller multiplication of the compensation capacitor. The second stage common-mode feedback circuit senses the output common-mode voltage with a switched-capacitor network similar to that used in the first stage common-mode feedback. The output common-mode voltage is then used to control two common-source amplifiers that drive the output nodes.

The two one-bit quantizers in the modulator of Fig. 6 are realized using the low power, dynamic comparator illustrated in Fig. 11 [8]. Transistors M_3 and M_4 serve to break the current path between the supplies once a decision has been made. They also provide some measure of isolation from kickback into the inputs during regeneration. The outputs of the comparators are stored in SR latches, the outputs of which are buffered and drive a switch network connected to the feedback reference voltages.

This design requires feedback reference voltages that are equal to the supply voltages since lowering the feedback levels reduces the dynamic range proportionally. The reference voltages must be conditioned so that they do not introduce noise into the modulator. If the references are generated on-chip, a supply independent circuit that can provide a voltage close to V_{DD} should be used.

In 5-V circuits, rail-to-rail operation of analog switches can be achieved through the use of CMOS switches in which the NMOS and PMOS devices are driven by complementary control signals. The maximum on-resistance of a CMOS switch occurs when input level is near midsupply. As the supply voltage is reduced, this maximum on-resistance increases quickly. In order to guarantee an adequately low switch resistance a low voltage environment, the clock voltage used to drive at least one of the two switch transistors can be bootstrapped beyond the supply voltage range. Shown in Fig. 12 is a circuit that can be used to boost the signal driving the NMOS switch transistors above V_{DD} [8]. Capacitors C_1 and C_2 are charged to V_{DD} via the cross-coupled NMOS transistors M_1 and M_2. When the input clock, CK, goes high, the output voltage, CK_{sw}, approaches $2V_{DD}$. The output voltage does not actually reach $2V_{DD}$ because of charge sharing with parasitic capacitances to ac ground. To avoid charge sharing with the large well parasitic, and to reduce the potential for latch-up, the well of the PMOS transistor M_3 is tied to an on-chip voltage doubler. Capacitor C_1 can be relatively small as it only drives the gate of a single NMOS transistor, M_2. However, capacitor C_2 must be large to boost the gates of many NMOS switch transistors, as well as wiring parasitics. In the experimental modulator, a boosted clock voltage of 3.3 V was obtained when operating from a 1.8-V power supply. The well of the PMOS switch is biased by the circuit shown in Fig. 13. This circuit produces a voltage of $2V_{DD}$ while consuming only a few microwatts of power.

A circuit schematic for the first stage of the cascaded modulator is shown in Fig. 14. The modulator is controlled by two-phase, non-overlapping clocks together with delayed versions of these clocks. Because of the low input common-mode voltage of 400 mV used for each of the integrators, switches S3, S4, S7 and S8 are simply NMOS transistors. However, because of the large signal swings in the first stage of the modulator, switches S1, S2, S5 and S6 are full CMOS transmission gates. All switches in the second stage of the modulator are NMOS transistors. In the switches S1 and S2, which sample the input and the feedback references in the first integrator, it is important to maintain a relatively constant resistance with variations in the voltage being sampled in order to avoid signal dependent charge injection [17]. This was accomplished by making the PMOS transistors in those switches 2.5 times larger than the NMOS transistors. While this does not fully equalize the on-resistance of the two transistors, it significantly reduces the variation. Larger switch sizes at the input have the disadvantage of increased kickback into the input signal source, which may have difficulty absorbing the charge.

IV. Experimental Results

The modulator of Fig. 6 has been integrated in a 0.8-µm, 5-V CMOS technology with metal-to-polycide capacitors. The performance of the design was assessed by driving it with a fully-differential sinusoidal signal, acquiring the digital outputs from the two stages with a custom test board, then transferring the data to a workstation for subsequent signal processing. Digital filtering and signal analysis were performed using the program MIDAS [15].

A die micrograph of the experimental modulator is shown in Fig. 15. The clocks are brought on chip as differential, low-swing voltages, and the two one-bit digital outputs are driven off chip as differential currents. Separate digital and analog ground planes were used on the test board and tied together at the power supply. The feedback references were brought on-chip via dedicated pins and tied to analog power and ground off chip. The common-mode level of the input source was tied to the midsupply voltage of the analog supplies, and the analog input, the feedback references, and the integrator outputs were all referenced to the same midsupply voltage.

When operated from a 1.8-V supply, the modulator's power dissipation, excluding the output drivers, is 2.5 mW. At a sampling frequency of 4 MHz with an oversampling ratio of 80, the corresponding Nyquist sampling rate is 50 kHz and the signal bandwidth is 25 kHz. Plots of the SNR and SNDR versus input amplitude are shown in Fig. 16. To generate these plots, the amplitude of the sinusoidal signal source was stepped in 1-dB increments from 0 dB to –85 dB. At each step, an FFT was taken and the SNR and SNDR were recorded. The curves are extrapolated from –85 dB to the noise floor of the modulator. The overload level of the modulator is –1 dB below the differential reference voltage of $2V_{DD}$. Thus, the full-scale differential input range is 3.2 V. From Fig. 16 it is apparent that for digital audio bandwidths the modulator achieves a dynamic range of 99 dB and a peak signal to noise plus distortion ratio of 95 dB when operated from a 1.8-V supply. The measured performance of the modulator is summarized in Table 2. The results of simulations predicting the performance of the amplifier are summarized in Table 3.

Because sampling and amplifier noise introduced in the second and third integrators is shaped, it is possible to significantly reduce the capacitor sizes in these circuits. In the experimental prototype, this scaling is very conservative and the combined power dissipation of the second and third integrators was lowered to only slightly less than that of the first integrator. More aggressive scaling could further lower the modulator power dissipation.

Fig. 17 plots an FFT of the output spectrum for a –20 dB, 2-kHz test signal. The frequency independence of the noise floor indicates that the modulator's performance is limited by thermal, rather than quantization, noise. Fig. 18 plots the dynamic range of the modulator as a function of oversampling ratio for a sampling rate of 4 MHz. While in a quantization noise limited third order modulator, the dynamic range increases by 21 dB/octave increase in oversampling ratio, in the thermal noise limit, the increase is only 3 dB/octave. For oversampling ratios below 64, the modulator is quantization noise limited, and for oversampling ratios above 64, it is thermal noise limited.

Fig. 19 plots the measured dynamic range and power dissipation as a function of the supply voltage for a signal bandwidth of 25 kHz and an oversampling ratio of 80. The modulator operates successfully for supply voltages ranging from 1.5 V to 2.5 V. The minimum supply voltage is limited by the input stage of the operational amplifiers, while the maximum supply voltage operation is limited by the oxide stress produced by the voltage doublers. The dynamic range improves with higher supply voltages due to increased signal power and a constant thermal noise floor. Below a supply voltage of 1.6 V, the modulator resolution falls off quickly due to charge loss at the integrator inputs brought about by a slight forward biasing of the switch source/drain junctions that results from transient voltage spikes. Since the bias currents are held constant and the power dissipation is dominated by the analog circuits, the power dissipation increases linearly with supply voltage.

An important phenomenon that can degrade the performance of sigma-delta modulators is the presence of spurious noise tones in the baseband output spectrum [11]. Previous work has shown that cascaded modulator architectures can be designed to be free of this problem [14]. Fig. 20 plots the maximum baseband tone peak that results from a dc input as a function of the dc input level. To generate the plots of Fig. 20, the dc input was stepped in fine increments over the input range from zero to the maximum positive input for both an experimental modulator and a simulation. Results for the negative half of the input range are symmetric about the zero input. At each dc input value, an FFT was taken and the power of the maximum baseband noise peak was recorded. For dc levels near the zero input the output spectrum is free of tones. For dc inputs below –1.1 dB of full scale, the strongest tone in the measured data is less than the thermal noise floor of –100 dB.

The power efficiency of various A/D converters with different resolutions and Nyquist sampling rates can be compared using the following figure of merit,

$$FM = \frac{4kT \times DR \times f_N}{P} \quad , \tag{10}$$

where *P* is the total power dissipation of the converter and *DR* is expressed as a ratio rather than in dB. This figure of merit is defined so that *FM*=1 for an integrator implemented with an ideal class B amplifier. Fig. 21 plots *FM* for some recently published CMOS A/D converters [1], [4]-[9], [14], [18]-[22]. The power dissipation used to compute *FM* does not include the decimation filter in the case of oversampling converters, nor does it account for the antialiasing filter in Nyquist rate converters. As expected from the discussion in Part B of Section II, the dependence of the figure of merit on conversion rate becomes quadratic for faster, lower resolution converters.

V. Conclusion

It has been shown that switched-capacitor circuits are a viable approach to the design of low-voltage, high-resolution sigma-delta modulators, even when only high threshold voltage transistors are available. It has been noted that the reduction of the oversampling ratio has limited benefit for the reduction of the modulator power dissipation. Furthermore, a reduction in supply voltage will generally increase the power dissipation in high-resolution analog circuits. In the experimental sigma-delta modulator described herein, low voltage operation has been achieved by using switched-capacitor integrators that employ a two-stage class A/AB operational amplifier with different input and output common-mode voltage levels. A boosted clock driver is used to maintain a low on-resistance for the analog switches. The switches at the amplifier inputs can be implemented with single NMOS transistors owing to the use of a low common-mode input level. CMOS transmission gates are used for switches that undergo large signal excursions. Low power dissipation has been obtained by designing a thermal noise limited modulator with a high input overload level with respect to the feedback reference voltages, which are tied to analog power and ground. The use of high swing amplifiers and signal scaling prevents clipping at the integrator outputs.

APPENDIX

This Appendix presents a derivation of the results given in (4) and (5) for the power dissipation in ideal integrators of the form shown in Fig. 2. First, an integrator implementation with an ideal class A amplifier is considered, then one with an ideal class B amplifier. The amplifiers are assumed to be noiseless, have infinite gain and bandwidth, and contribute no parasitic capacitances.

The dynamic range (*DR*) of a modulator for which the resolution is limited by the *kT/C* noise of the first integrator, given in (3) and repeated here for convenience, is

$$DR = \frac{S_S}{S_{kT/C}} = \frac{V_{sw}^2 M C_S}{8kT} \quad . \tag{11}$$

From this expression if follows that

$$C_S = \frac{8kT(DR)}{MV_{sw}^2} \quad . \tag{12}$$

The average power dissipation of the integrator is

$$P = I_{amp} V_{DD} \quad , \tag{13}$$

where I_{amp} is the average amplifier current and V_{DD} is the supply voltage. In a class A amplifier the quiescent amplifier current is also the maximum current which can be delivered to the load. Therefore, the quiescent current must be high enough so that the load can be charged to the worst case output voltage step within the integration period. Thus,

$$I_{amp} = \frac{C_I \Delta V_{out}}{T_S/2} \quad , \tag{14}$$

where ΔV_{out} is the worst case differential step change in the output voltage, and T_S is the clock period. The factor of 2 accounts for the fact the integration must normally be completed in half the clock period. ΔV_{out} can be expressed as

$$\Delta V_{out} = (V_{sw} + V_{ref}) \frac{C_S}{C_I} \quad , \tag{15}$$

where V_{ref} is the differential amplitude of the feedback reference voltage of the modulator. T_S can be expressed as

$$T_S = \frac{1}{f_S} = \frac{1}{Mf_N} \quad , \tag{16}$$

where f_S is the sampling frequency, f_N is the Nyquist sampling rate, and M is the oversampling ratio. By substituting (15) and (16) in (14), the expression for I_{amp} can be rewritten as

$$I_{amp} = 2C_s Mf_N (V_{sw} + V_{ref}) \quad . \tag{17}$$

From (12), (13) and (17), it follows that the power dissipation can be expressed as

$$P = 16kT(DR)f_N \frac{V_{DD}(V_{sw} + V_{ref})}{V_{sw}^2} \quad . \tag{18}$$

If it is further assumed that V_{sw} and V_{ref} are full rail signals, (18) reduces to (4), namely

$$P = 32kT(DR)f_N \quad . \tag{19}$$

In a class B amplifier, the quiescent power consumption is zero. Power is consumed only when the output voltage changes. It can be shown that the average power dissipation of a fully differential integrator implemented with an ideal class B amplifier is

$$P = \frac{1}{2} C_I f_S V_{DD} \overline{\Delta V_{out}} \quad , \tag{20}$$

where $\overline{\Delta V_{out}}$ is the average differential output voltage step size, which is related to the average differential input voltage step size by

$$\overline{\Delta V_{out}} = \frac{C_S}{C_I} \times \overline{\Delta V_{in}} \quad . \tag{21}$$

Substituting (12), (16), and (21) into (20) results in

$$P = 4kT(DR)f_N \frac{\overline{\Delta V_{in}} V_{DD}}{V_{sw}^2} \quad . \tag{22}$$

If it is further assumed that V_{sw} is a full rail signal, (22) reduces to (5), namely

$$P = 4kT(DR)f_N \frac{\overline{\Delta V_{in}}}{V_{DD}} \quad . \tag{23}$$

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Figure Captions

Fig. 1 Simplified sigma-delta modulator block diagram.

Fig. 2 Switched-capacitor integrator with ideal amplifier.

Fig. 3(a) Folded cascode amplifier.

Fig. 3(b) Two-stage class A amplifier.

Fig. 3(c) Two-stage class A/AB amplifier.

Fig. 4 First integrator power dissipation vs. supply voltage.

Fig. 5 First integrator power dissipation vs. oversampling ratio.

Fig. 6 Sigma-delta modulator architecture.

Fig. 7 Operational amplifier.

Fig. 8(a) Ac differential-mode half-circuit.

Fig. 8(b) Simplified ac differential-mode half-circuit.

Fig. 9 Ac common-mode half-circuit.

Fig. 10 First stage common-mode feedback circuit.

Fig. 11 Dynamic regenerative latch.

Fig. 12 Boosted clock driver.

Fig. 13 Voltage doubler.

Fig. 14 First stage of modulator.

Fig. 15 Die micrograph of experimental modulator.

Fig. 16 Measured SNR and SNDR vs. input amplitude.

Fig. 17 Measured baseband output spectrum.

Fig. 18 Measured dynamic range vs. oversampling ratio.

Fig. 19 Measured dynamic range and power dissipation vs. supply voltage.

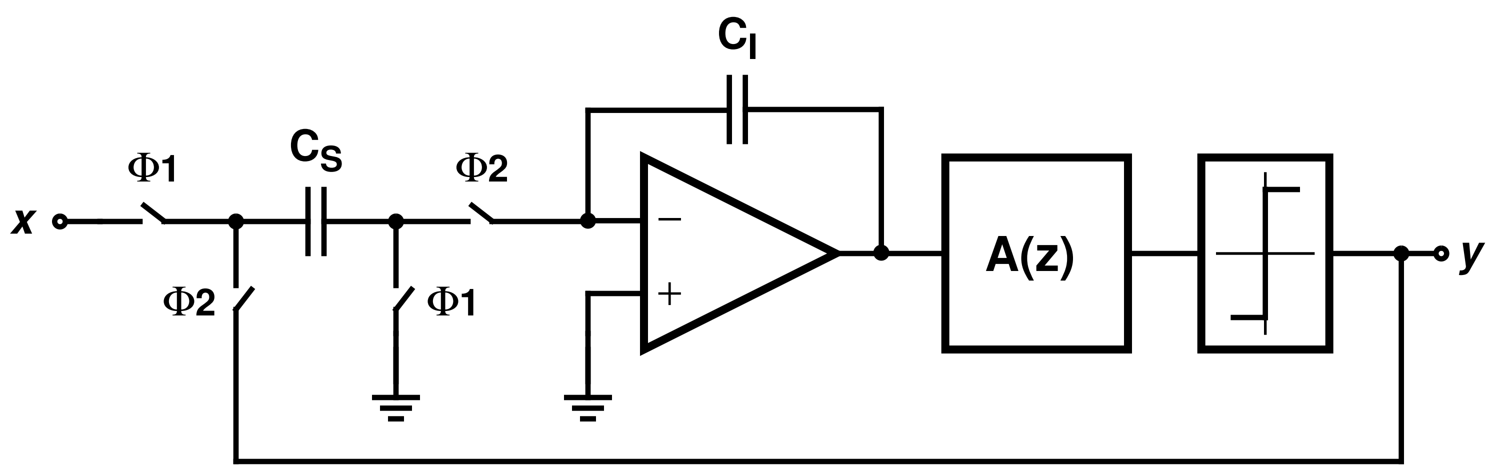


Fig. 1: Simplified sigma-delta modulator block diagram. (Rabii and Wooley)

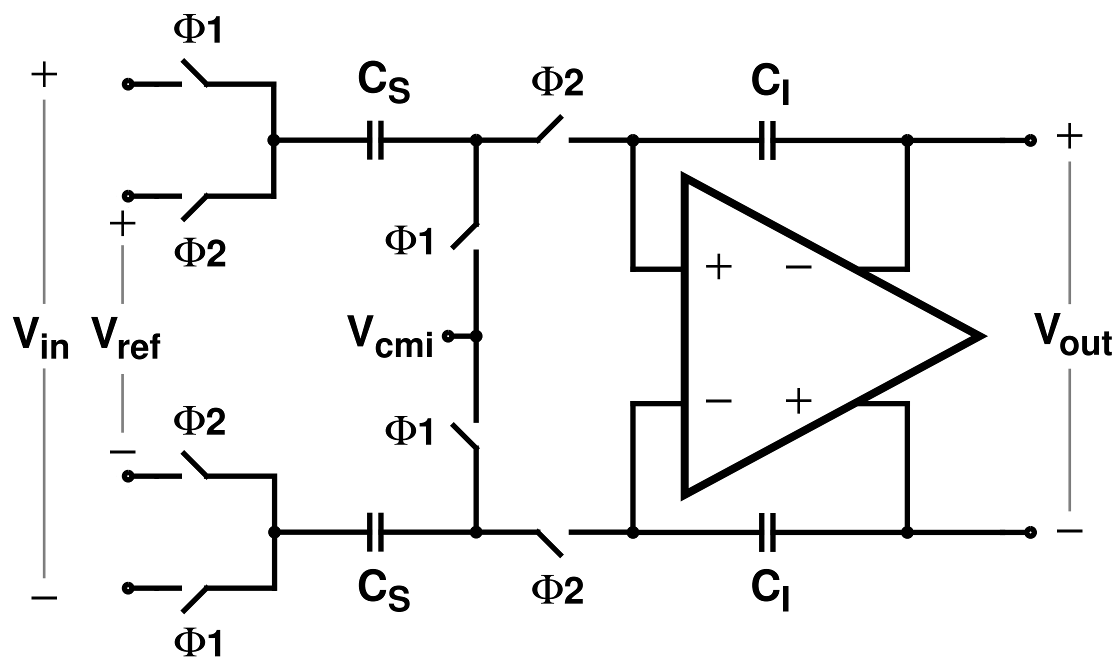


Fig. 2: Switched-capacitor integrator with ideal amplifier. (Rabii and Wooley)

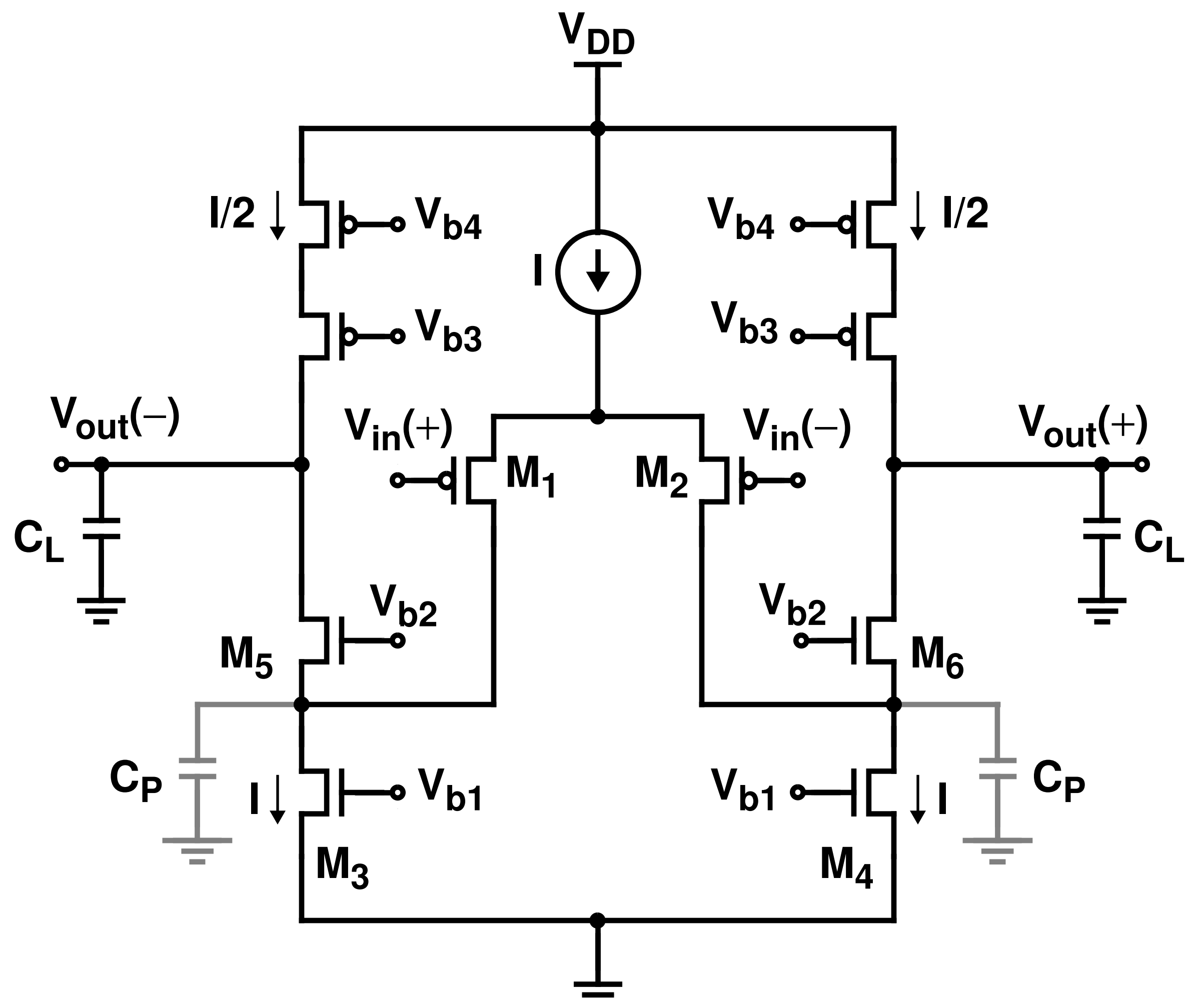


Fig. 3(a): Folded cascode amplifier. (Rabii and Wooley)

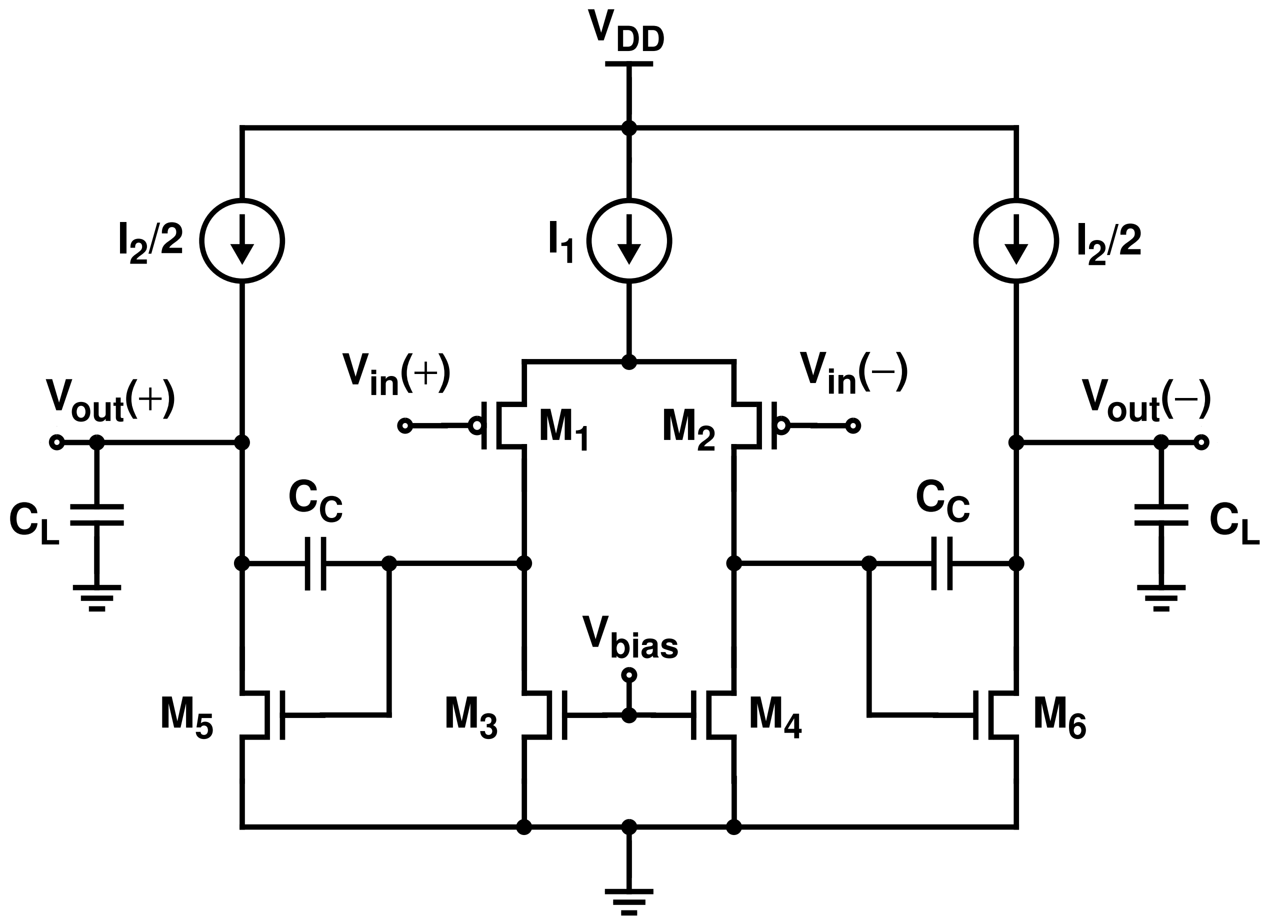


Fig. 3(b): Two-stage class A amplifier. (Rabii and Wooley)

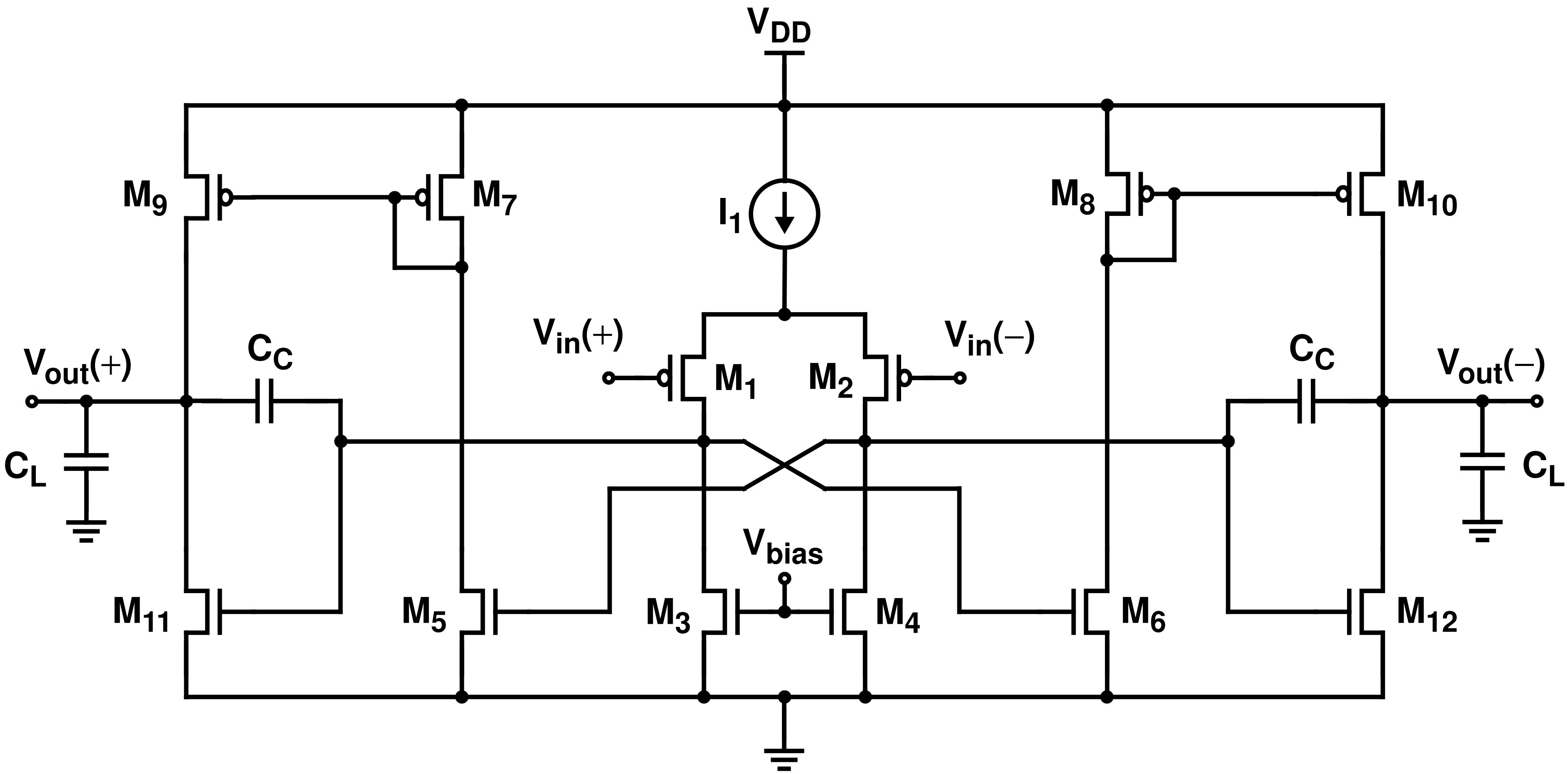


Fig. 3(c): Two-stage class A/AB amplifier. (Rabii and Wooley)

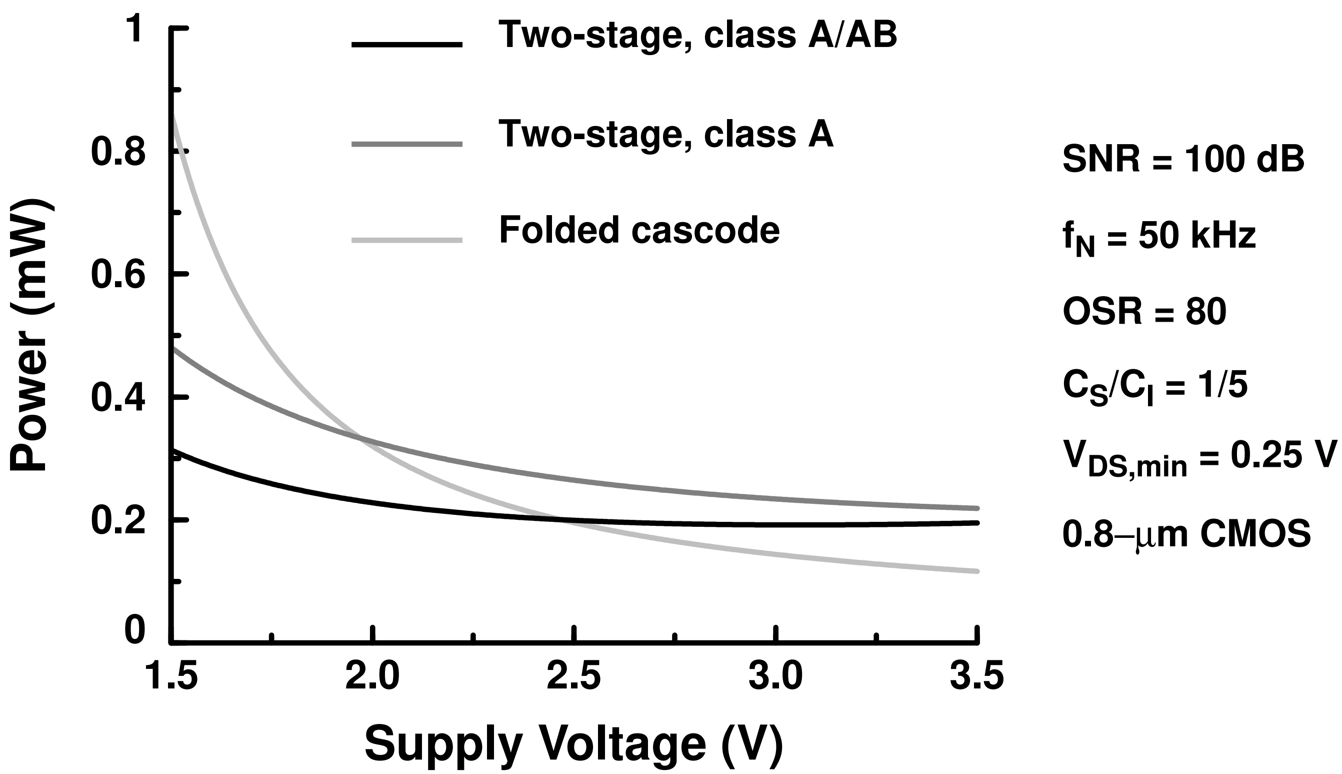


Fig. 4: First integrator power dissipation vs. supply voltage. (Rabii and Wooley)

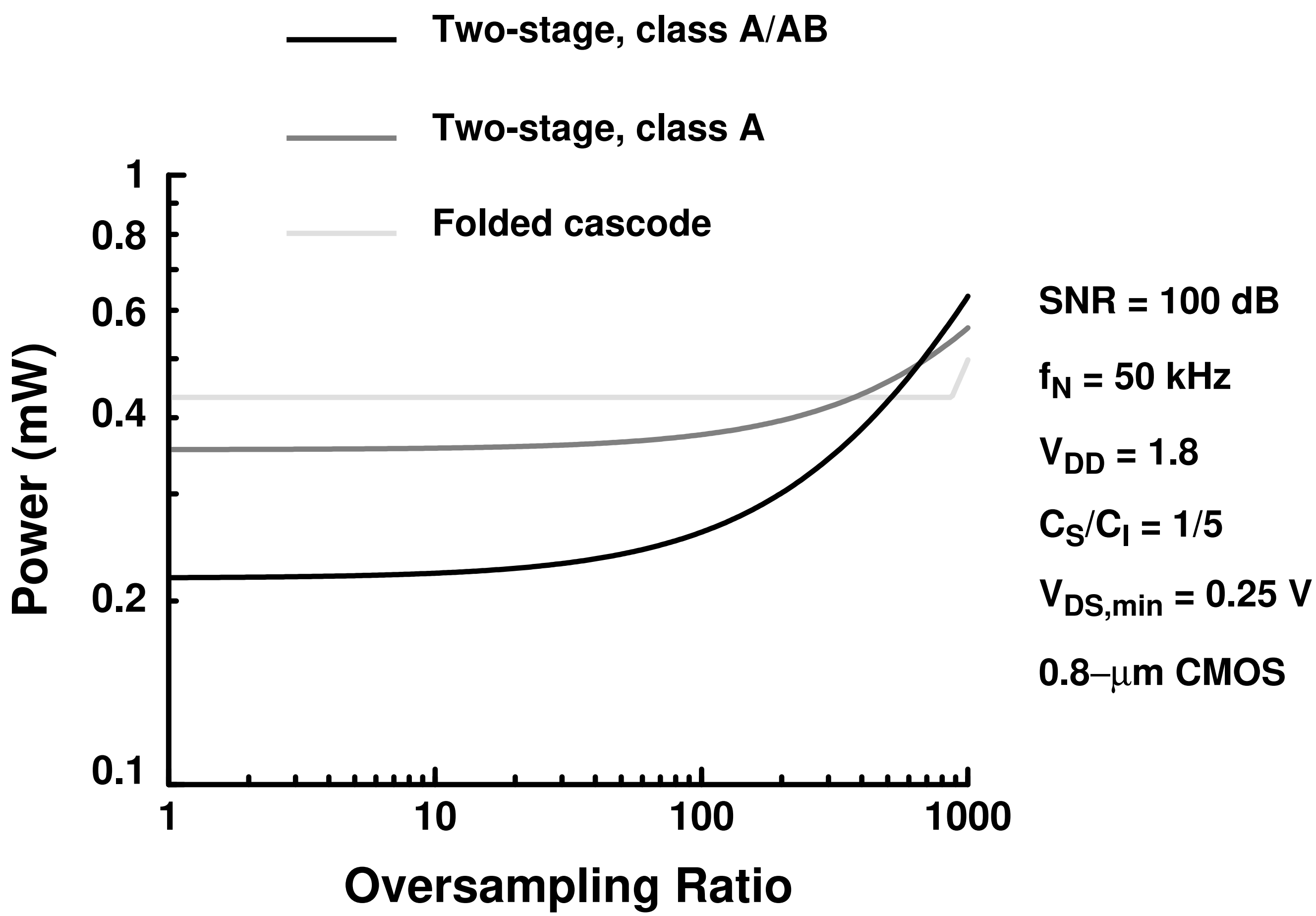


Fig. 5: First integrator power dissipation vs. oversampling ratio. (Rabii and Wooley)

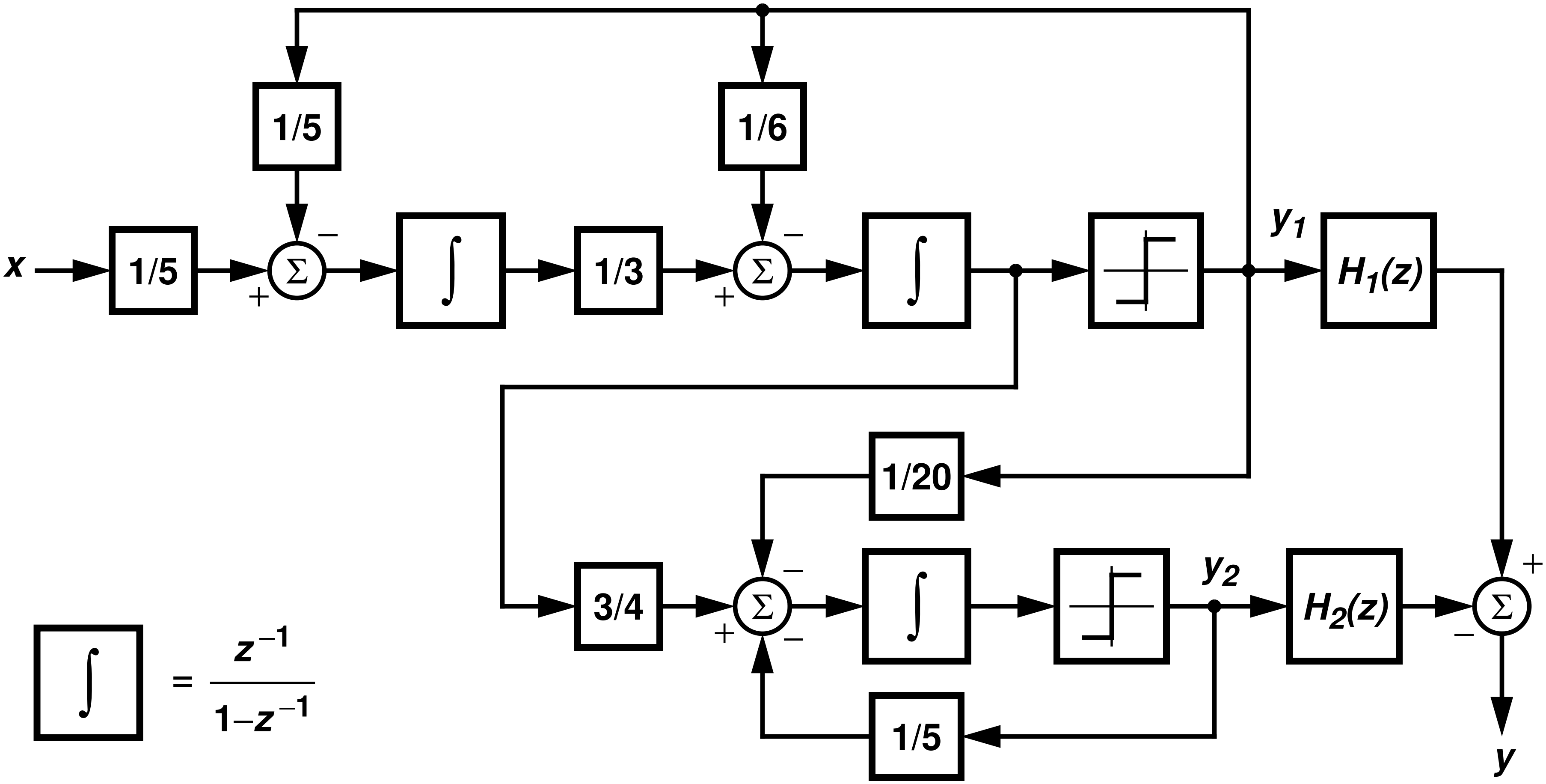


Fig. 6: Sigma-delta modulator architecture. (Rabii and Wooley)

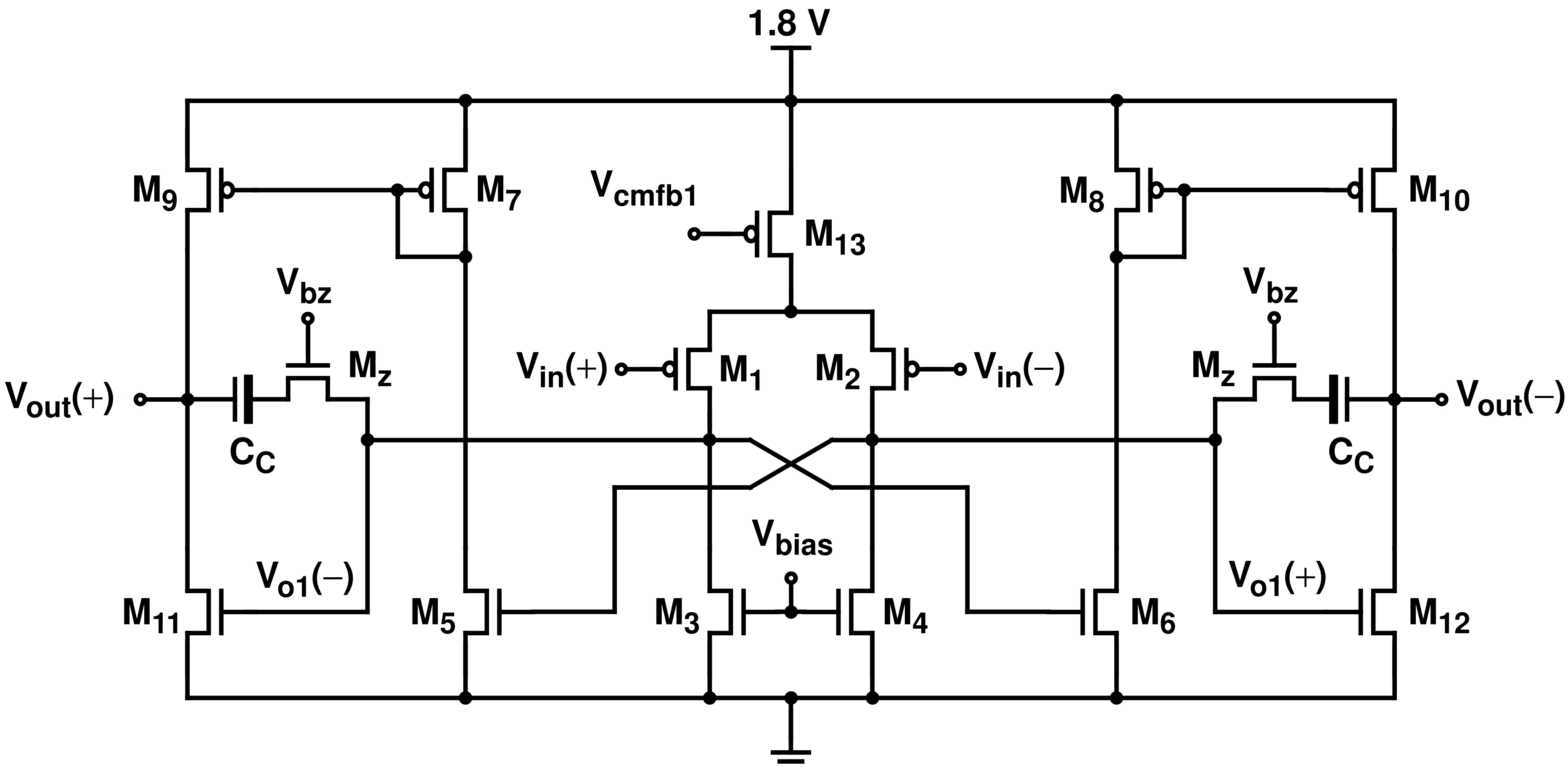


Fig. 7: Operational amplifier. (Rabii and Wooley)

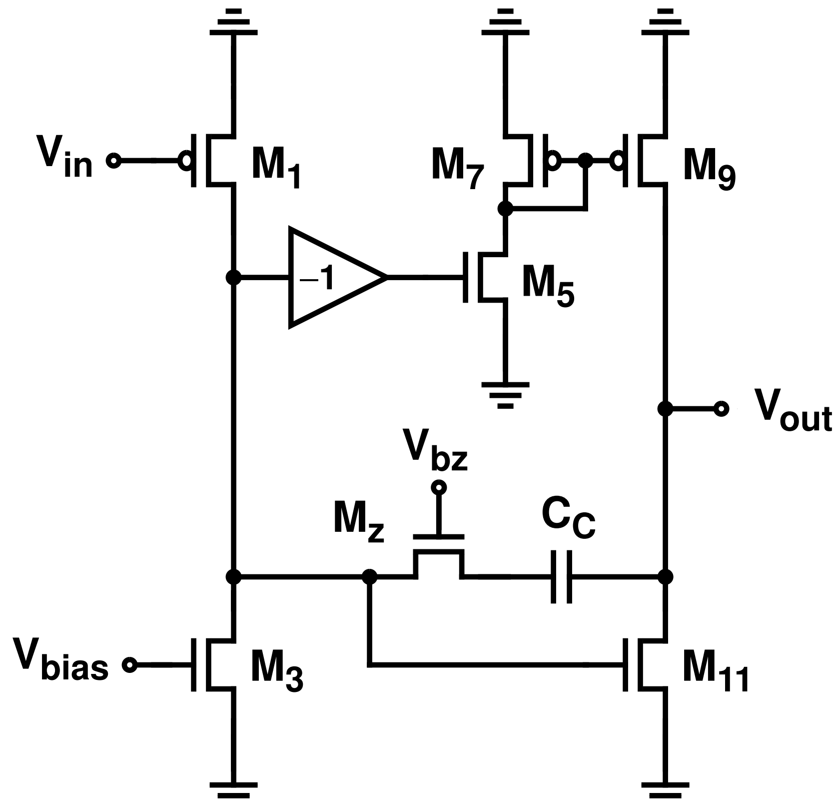


Fig. 8(a): Differential-mode half-circuit. (Rabii and Wooley)

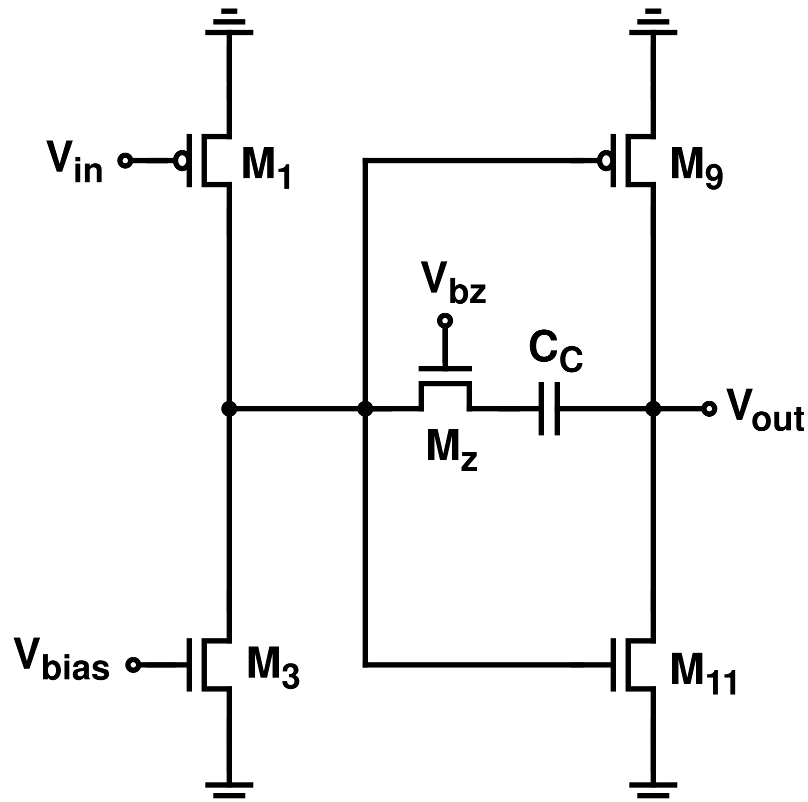


Fig. 8(b): Simplified differential-mode half-circuit. (Rabii and Wooley)

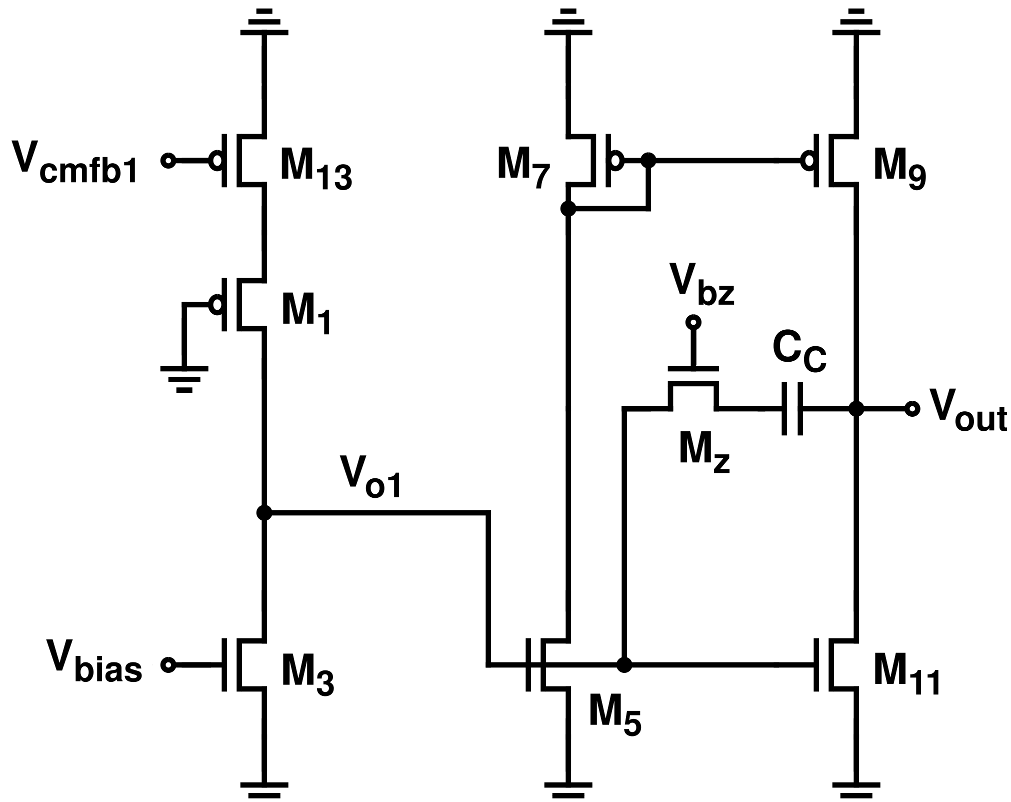


Fig. 9: Common-mode half-circuit. (Rabii and Wooley)

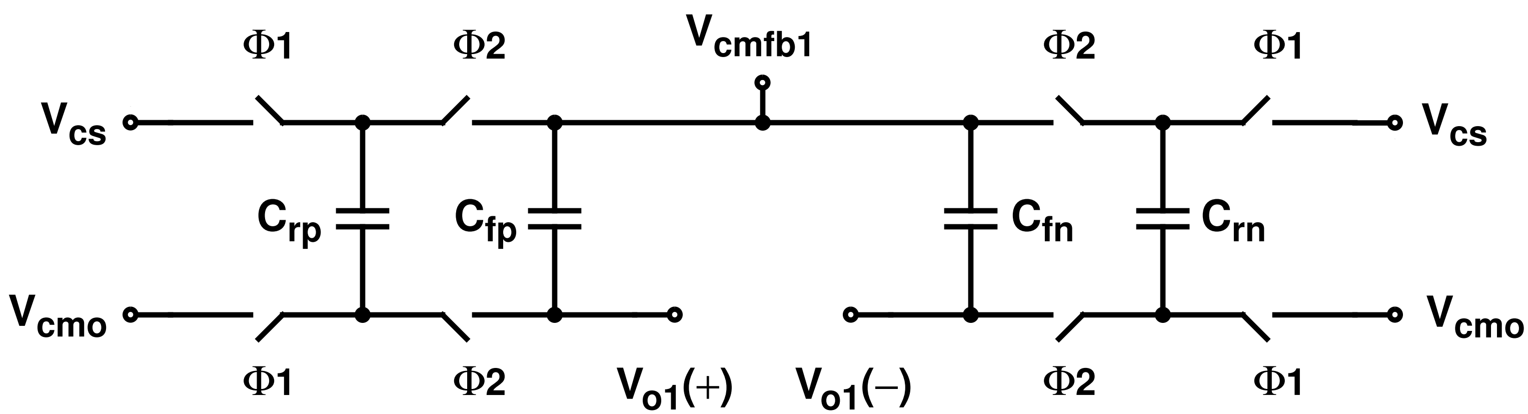


Fig. 10: First stage common-mode feedback circuit. (Rabii and Wooley)

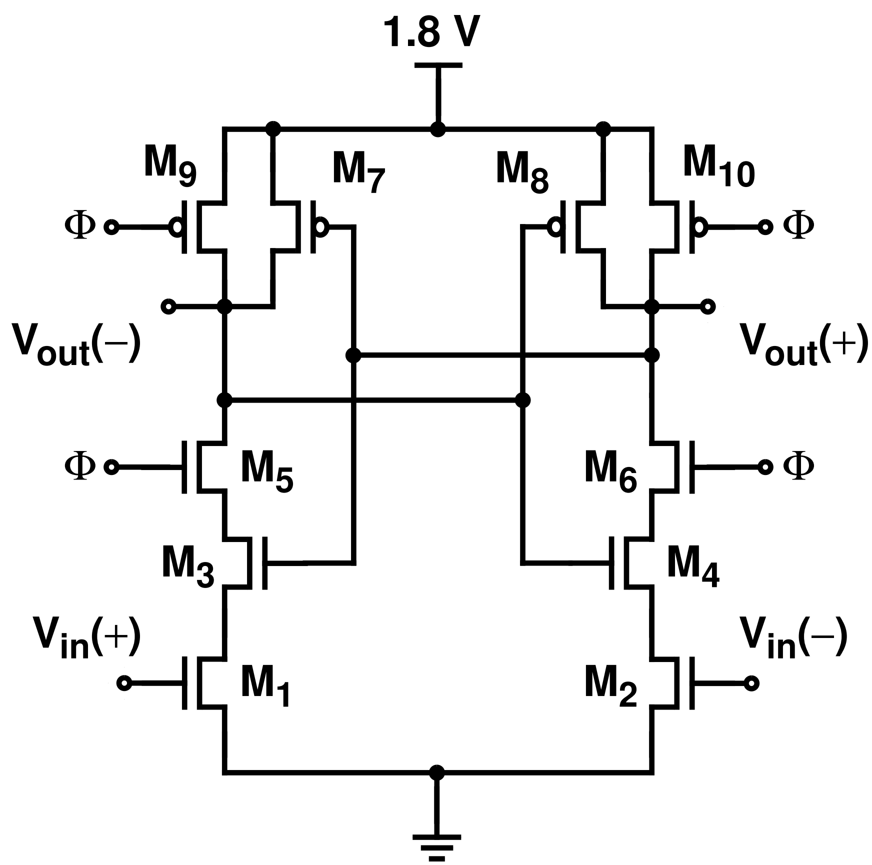


Fig. 11: Dynamic regenerative latch. (Rabii and Wooley)

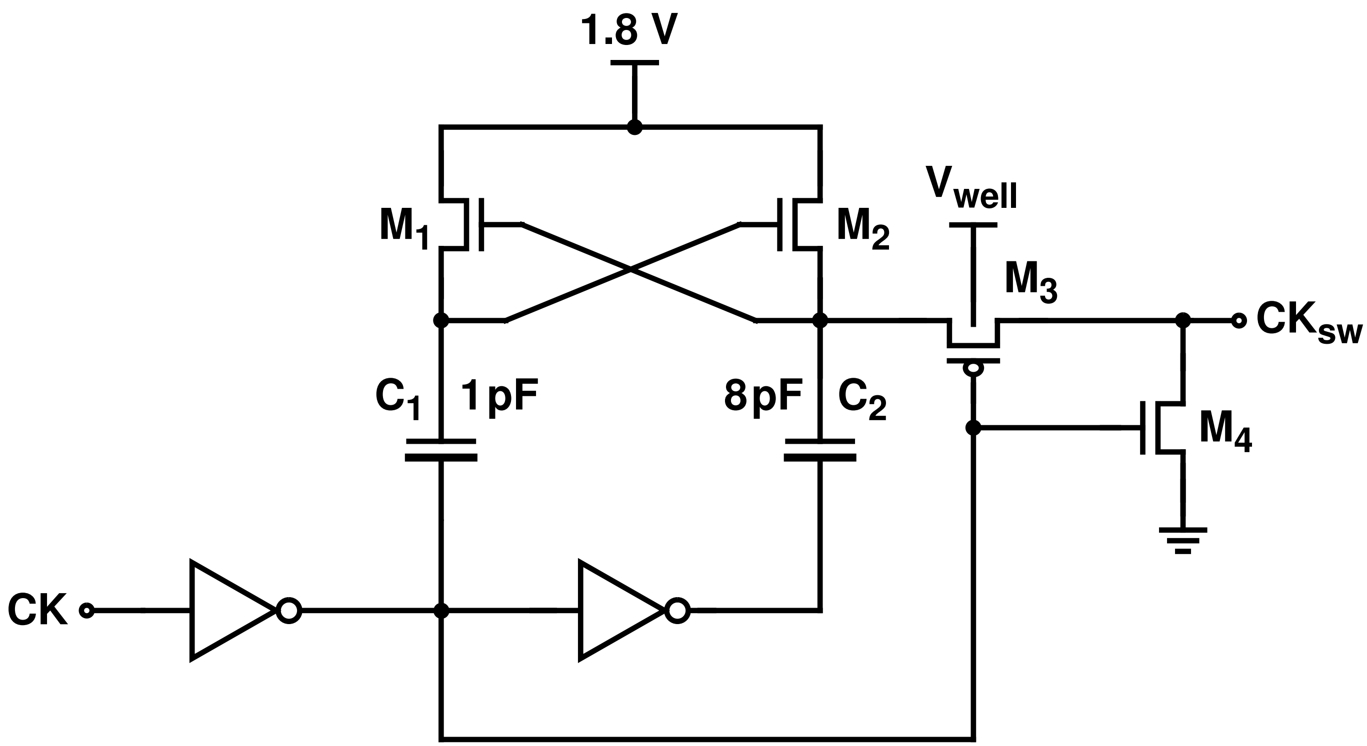


Fig. 12: Boosted clock driver. (Rabii and Wooley)

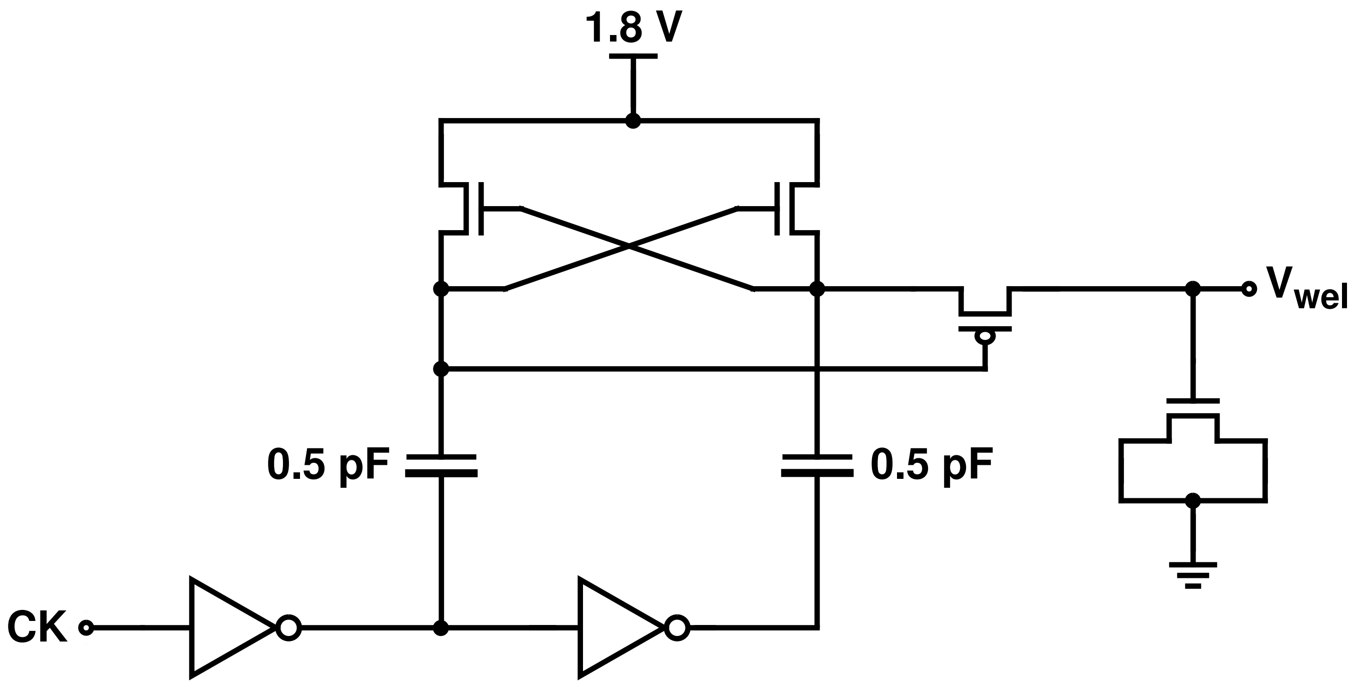
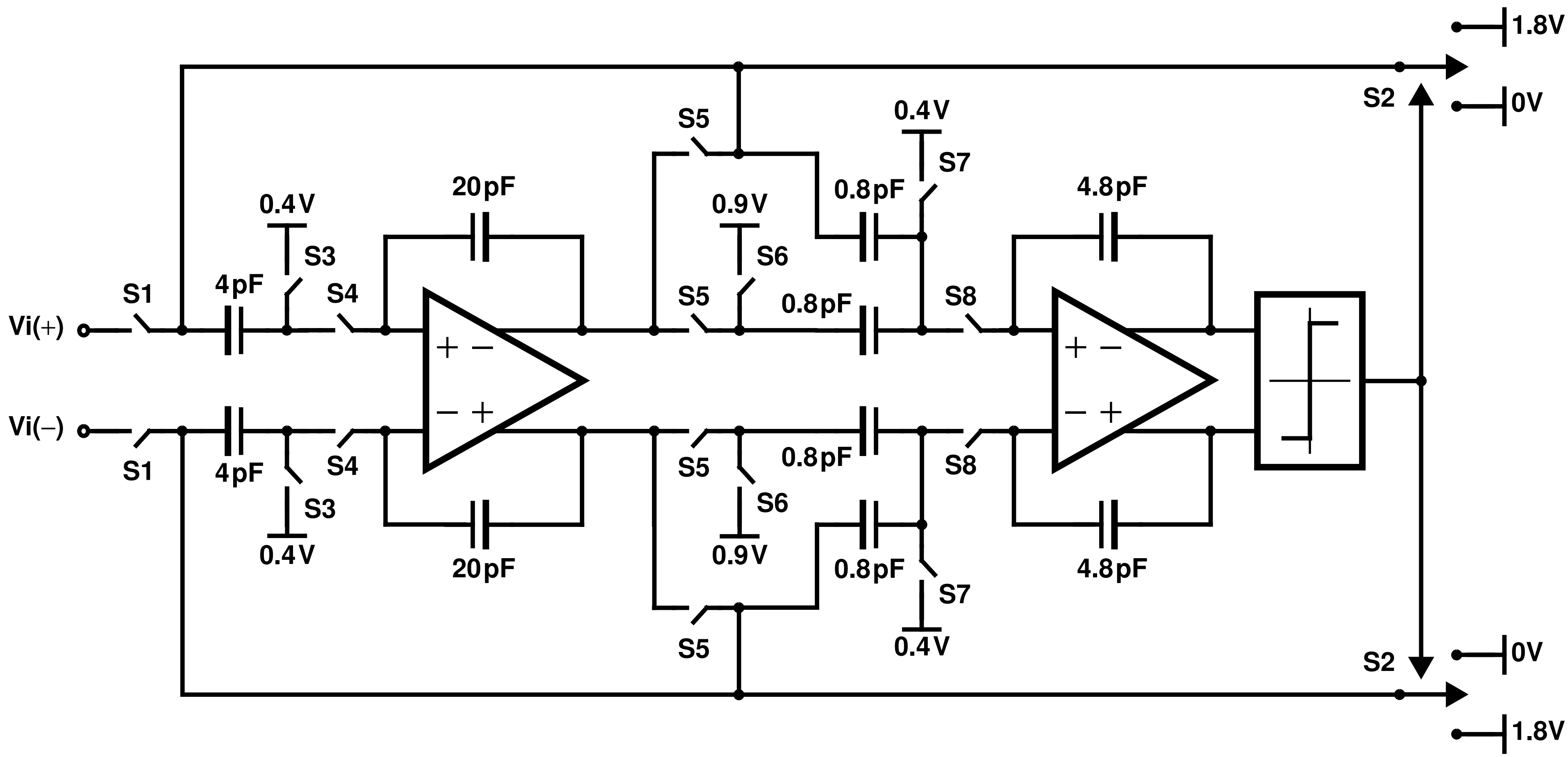


Fig. 13: Voltage doubler. (Rabii and Wooley)



S1, S5: $\Phi1_{delayed}$, CMOS   S3, S7: $\Phi1$, NMOS

S2, S6: $\Phi2_{delayed}$, CMOS   S4, S8: $\Phi2$, NMOS

Fig. 14: First stage of modulator. (Rabii and Wooley)

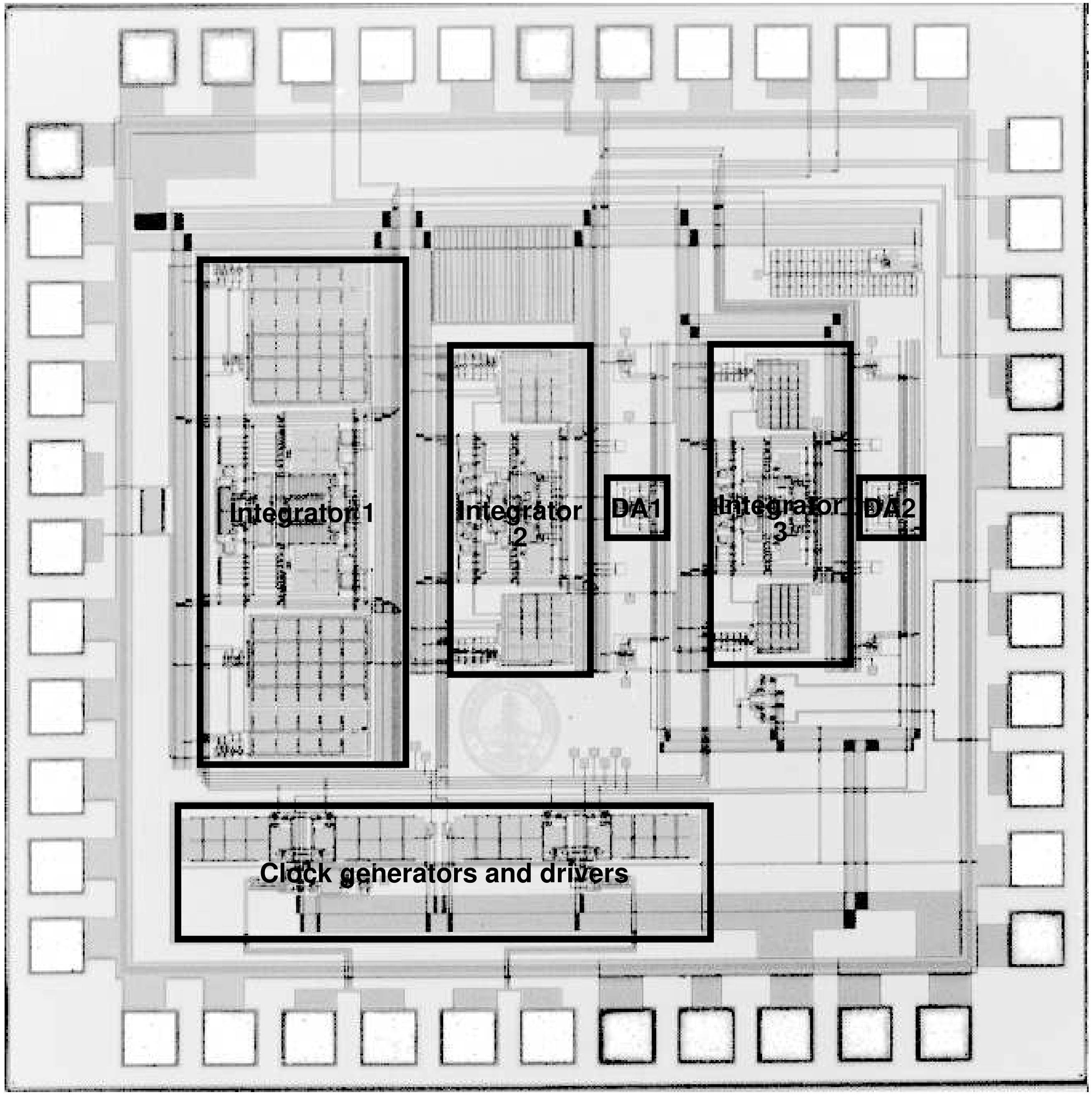


Fig. 15: Die micrograph of experimental modulator. (Rabii and Wooley)

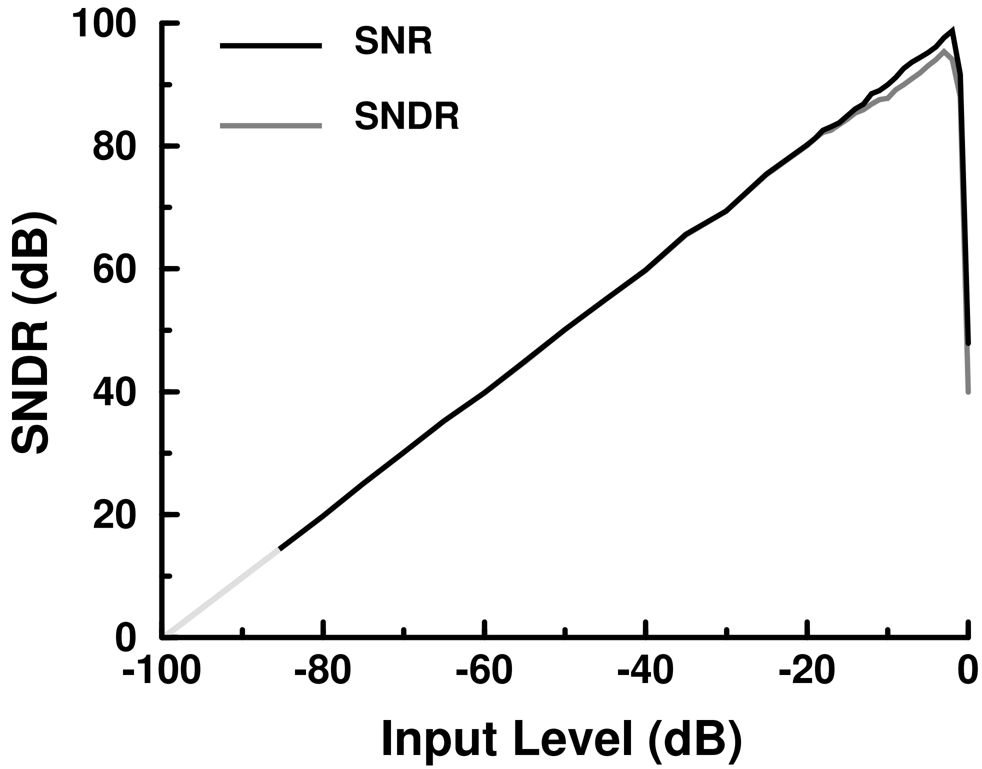


Fig. 16: Measured SNR and SNDR vs. input amplitude. (Rabii and Wooley)

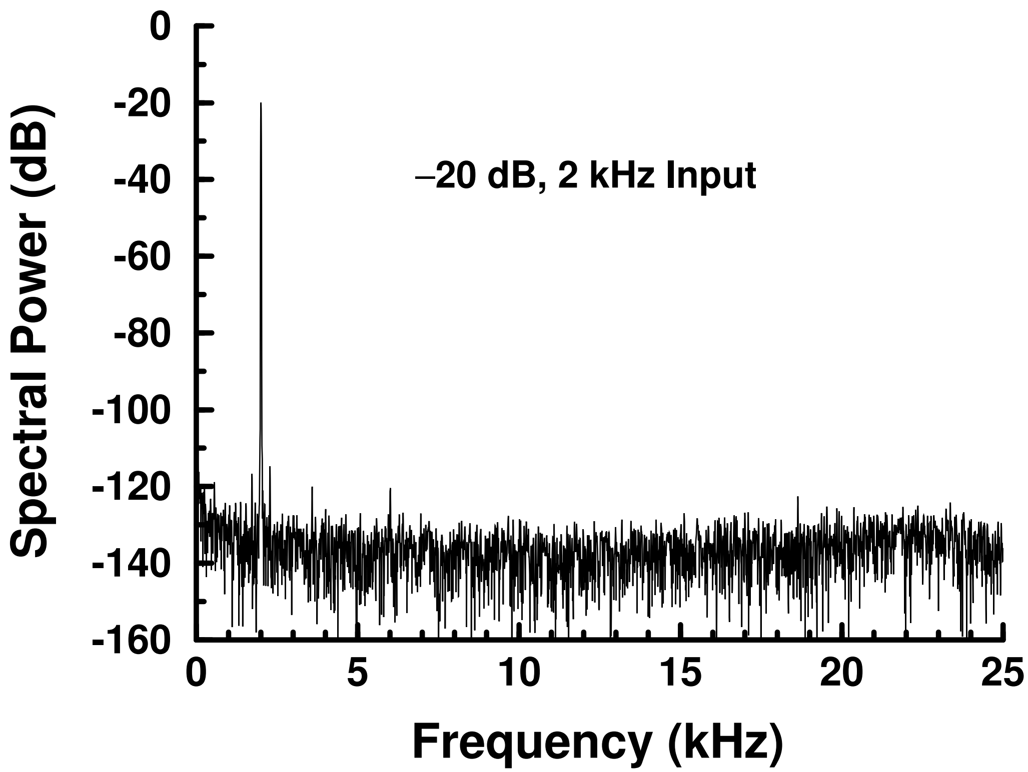


Fig. 17: Measured baseband output spectrum. (Rabii and Wooley)

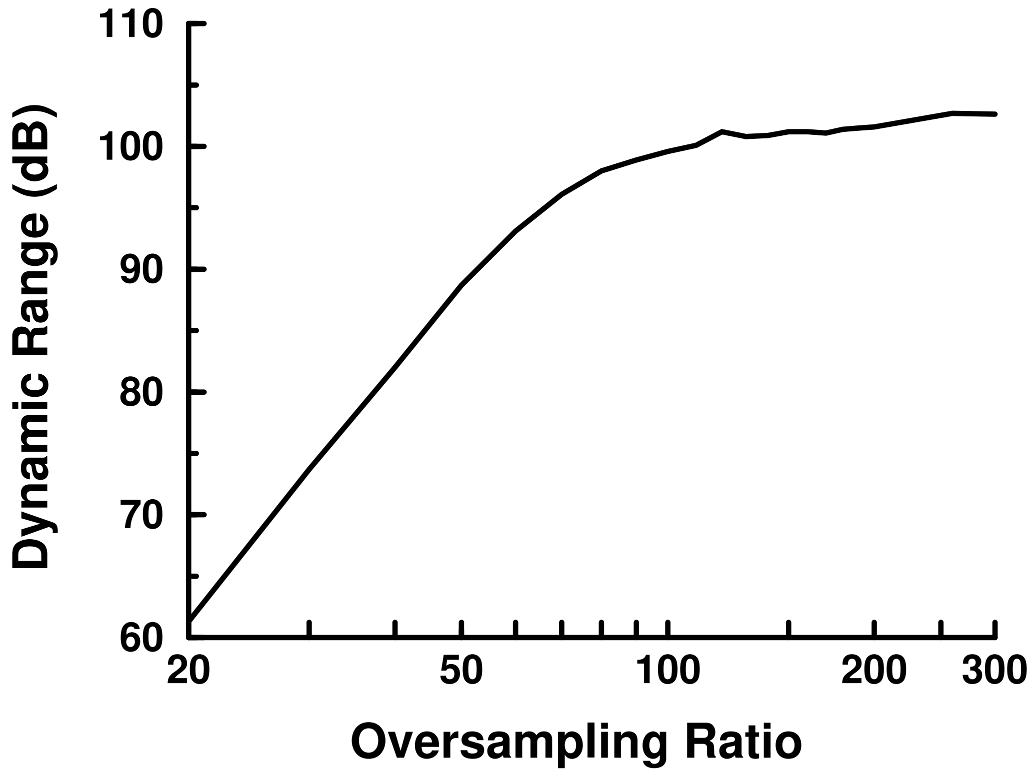


Fig. 18: Measured dynamic range vs. oversampling ratio. (Rabii and Wooley)

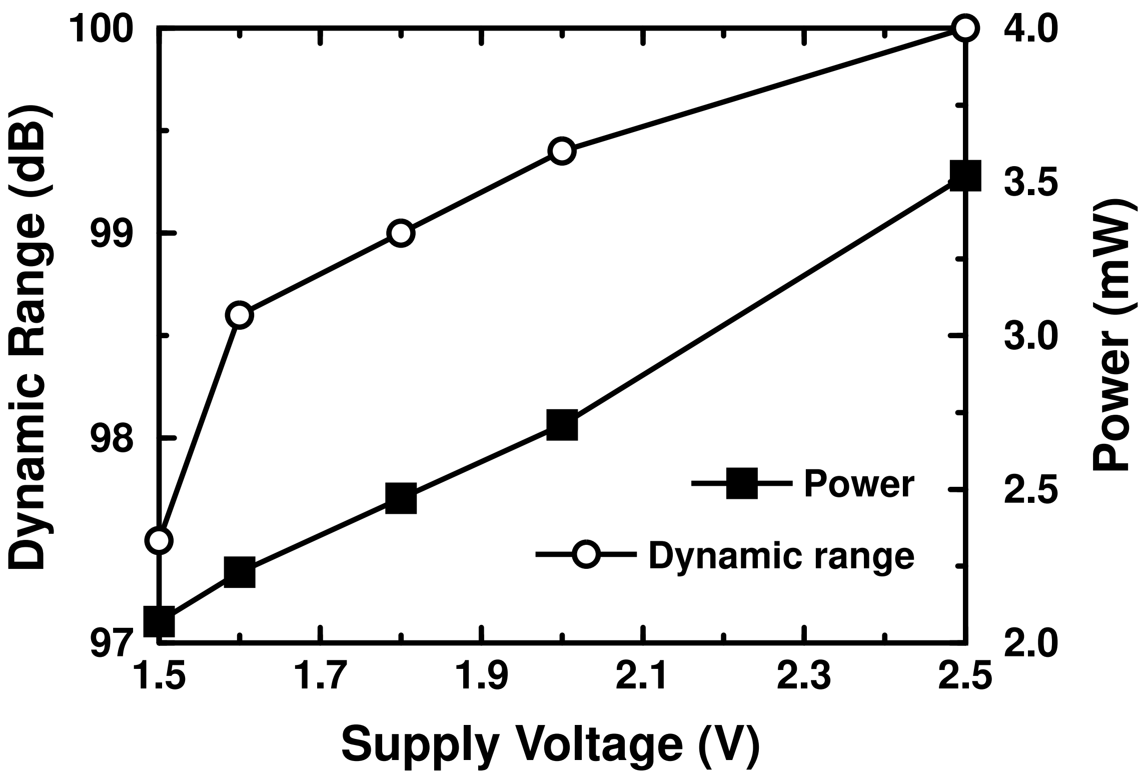


Fig. 19: Measured dynamic range and power dissipation vs. supply voltage. (Rabii and Wooley)

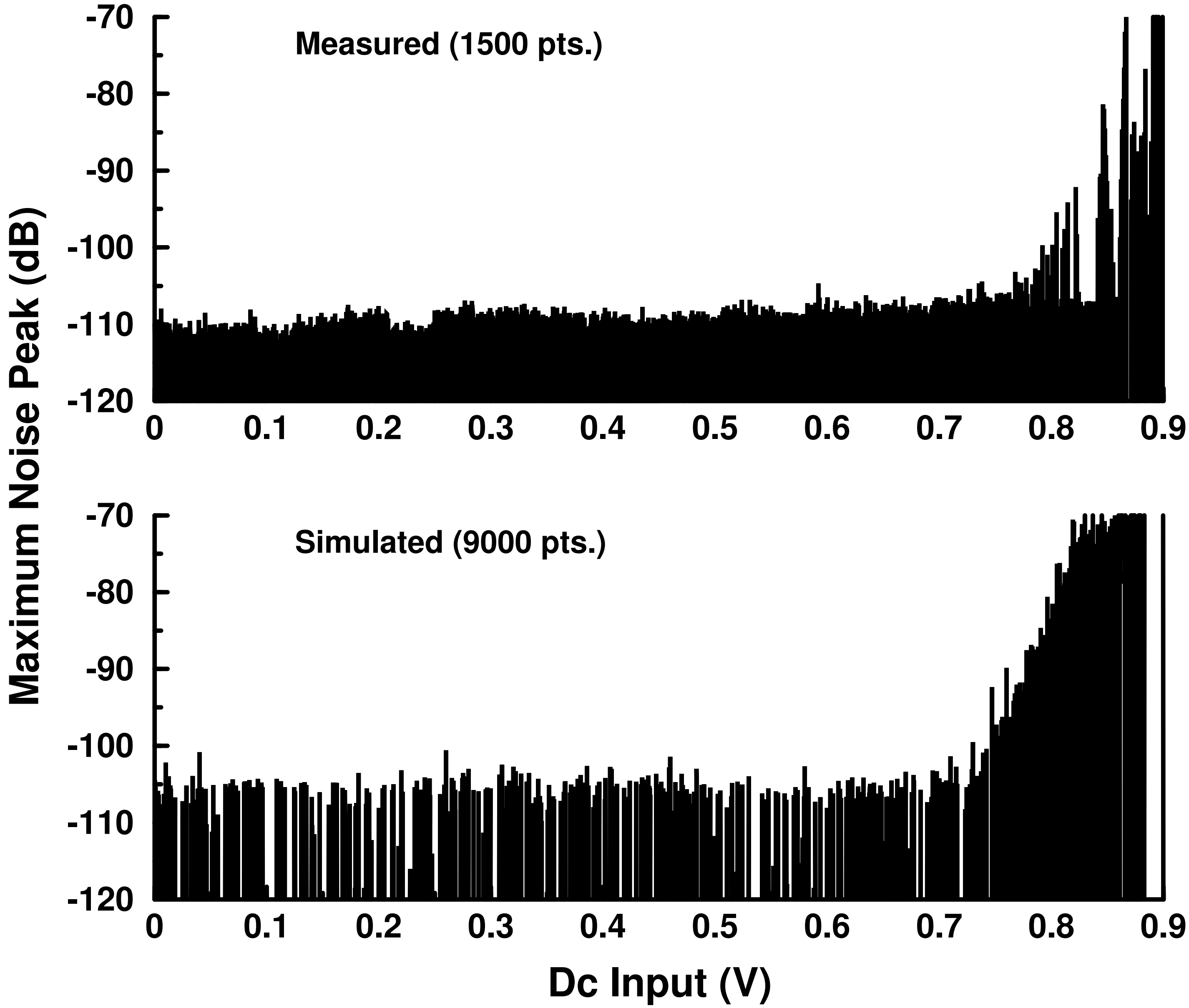


Fig. 20: Measured and simulated quantization tones. (Rabii and Wooley)

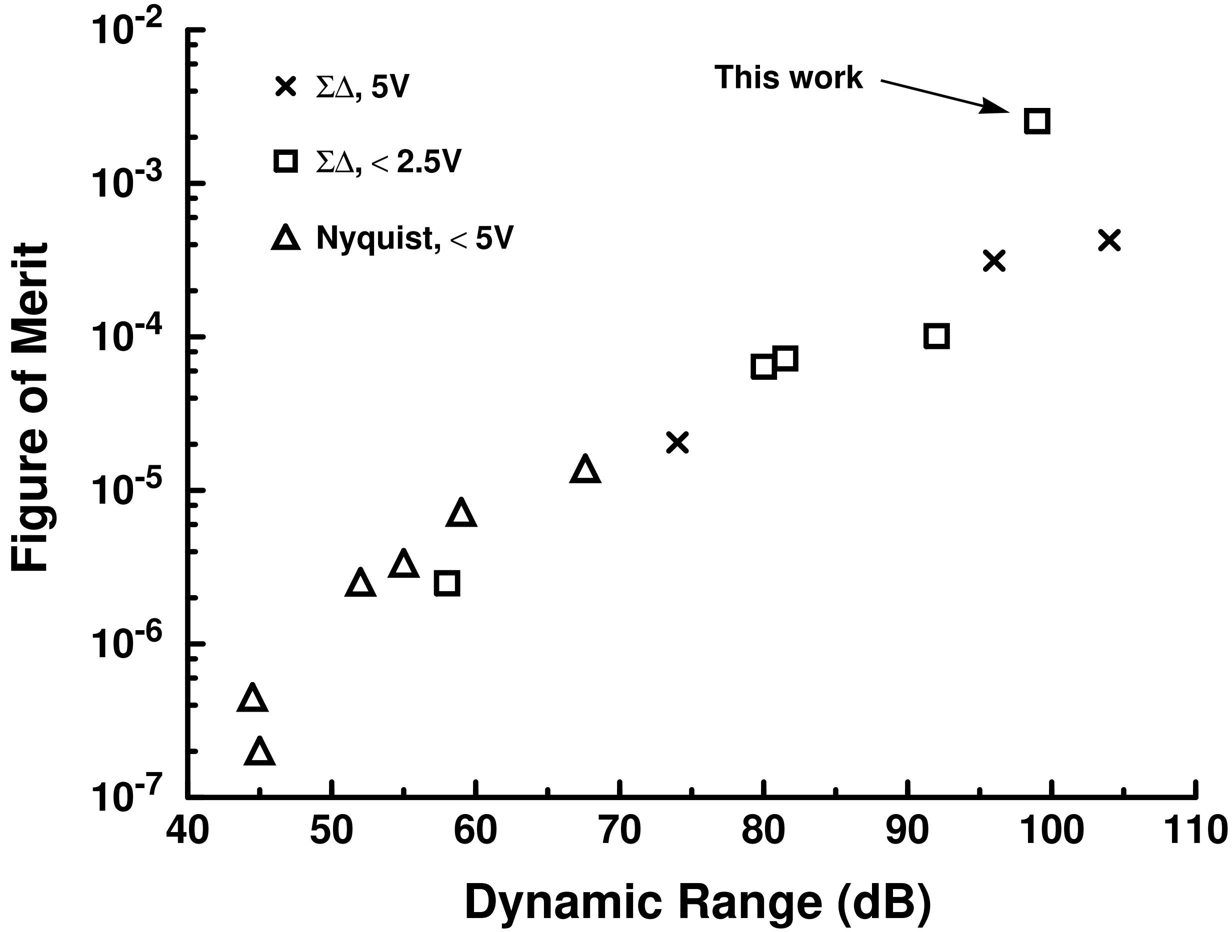


Fig. 21: Figure of merit vs. DR of recent analog-to-digital converters. (Rabii and Wooley)

Table 1: Key Parameters of Three Amplifier Topologies

Parameter	Folded Cascode	Two-Stage Class A	Two-Stage Class A/AB
Slew Rate	I/C_L	$\min(I_1/C_C, I_2/(C_L+C_C))$	I_1/C_C
Unity Gain Freq, ω_u	g_{m1}/C_L	g_{m1}/C_C	g_{m1}/C_C
Lowest Non-dominant pole, ω_2	g_{m5}/C_P	g_{m5}/C_L	$2g_{m11}/C_L$
Output Swing	$2V_{DD}-8\lvert V_{DS,min}\rvert$	$2V_{DD}-4\lvert V_{DS,min}\rvert$	$2V_{DD}-4\lvert V_{DS,min}\rvert$
Thermal Noise	$8\gamma kT/g_{m1}(1+g_{m1}/g_{m3}+g_{m1}/g_{m5})$	$8\gamma kT/g_{m1}(1+g_{m1}/g_{m3})$	$8\gamma kT/g_{m1}(1+g_{m1}/g_{m3})$
Minimum Supply	$\lvert V_{T1}\rvert+2\lvert V_{DS,min}\rvert$	$\lvert V_{T1}\rvert+2\lvert V_{DS,min}\rvert$	$\lvert V_{T1}\rvert+2\lvert V_{DS,min}\rvert$
CMRR	+	+	++
PSRR	+	–	++

Table 1: Key parameters of three amplifier topologies. (Rabii and Wooley)

Table 2: Modulator Performance Summary

Dynamic Range	99 dB
Peak SNR / SNDR	99 dB / 95 dB
Noise Floor	–100 dB
Overload Level	–1 dB
Sampling Rate	4 MHz
Oversampling Ratio	80
Signal Bandwidth	25 kHz
Power Supply Voltage	1.8 V
Total Power Dissipation	2.5 mW
First Integrator	1 mW
Active Area	1.5 mm^2
Technology	0.8-μm CMOS

Table 2: Modulator performance summary. (Rabii and Wooley)

Table 3: Simulated Operational Amplifier Performance

DC Gain	68 dB
Unity Gain Frequency	24 MHz
Settling Time Constant	10 ns
Slew Rate	14 V/μs
Linear Output Range	3 V

Table 3: Simulated operational amplifier performance. (Rabii and Wooley)