D. Shen, C.M. Hwang, B Lusignan, B.A. Wooley, "A 900 MHz Discrete-Time Filtering RF Front-End", 1996 Digest of Technical Papers , IEEE International Solid State Circuits Conference, Feb. 1996, San Francisco, CA.

# TP 3.4: A 900 MHz Integrated Discrete-Time Filtering RF Front-End

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Power, size, and cost are primary design considerations in radio receivers used for portable communications. Unfortunately, superheterodyne IC receiver designs require discrete tuned-circuits that consume valuable board space and dissipate significant amounts of power. Direct conversion receivers are an alternative to the superheterodyne receiver architecture [1]; however, in such receivers severe LO to RF leakage limits the achievable dynamic range [2]. Front-end A/D conversion is rarely a viable option because of its limited resolution and excessive power dissipation at high conversion rates.

This work introduces a radio receiver architecture that avoids the need for external intermediate frequency (IF) filters, while maintaining the selectivity required for narrowband frequency-multiplexed channels. The receiver is based on a subsampling architecture and operates in the 800-900 MHz frequency range. It is a potential candidate for use in applications such as portable mobile data systems, personal communications devices, and cordless telephony.

A block diagram of the proposed receiver is shown in Figure 1. This receiver differs from a superheterodyne architecture in that the mixer is replaced by a sampling circuit, and the intermediate frequency filters are replaced by a cascade of downsampling stages employing discrete-time filtering. The process of subsampling, sampling the input signal at a rate lower than the highest frequency components of the input signal, performs a function equivalent to mixing. Because the input is bandlimited by an analog RF filter, the Nyquist criterion is satisfied as long as the sampling rate is more than twice the magibandwidth of this filter. The noise filter following the low noise amplifier (LNA) limits the noise bandwidth so as to prevent wideband noise from aliasing into the signal band and increasing the noise floor.

Following sampling, the signal is filtered to select the desired baseband in the presence of interfering signals. This is accomplished by means of successive bandpass downsampling stages, with each stage consisting of an analog discrete-time filter followed by a sampling rate reduction. The filters prevent aliasing due to downsampling and provide a narrow bandpass function to select and amplify the desired signal. In order to keep the transfer function of the anti-aliasing filter relatively easy to implement, multiple stages each with a downsampling ratio of only 2 to 1 are used. A second-order biquadratic filter, with a single notch in the stopband, can then be used as an effective anti-aliasing filter. Because the downsampling process is accomplished with analog discrete-time filters, there is no quantization error. The dynamic range of the LNA, sample-and-hold amplifier, and first biquadratic filter determine the dynamic range of the system. The bandpass filter response of the system is tuned to a fixed ratio of the sampling rate. Thus, tuning is accomplished by simply adjusting the sampling rate, thereby changing the carrier frequency to sampling rate ratio. Once the sampling rate has been lowered significantly, the signal is digitized so that the channel-select filtering, demodulation, and baseband processing can be done digitally.

A prototype of the receiver front-end, excluding the LNA and noise filter, has been integrated in a 0.6-µm BiCMOS technology. A block diagram of this circuit is shown in . The circuit implements a 78-Msamples/sec front-end sample-and-hold circuit and three stages of 2-to-1 downsampling. The carrier frequency to clock frequency ratio is chosen so that an image of the desired channel falls at exactly one third the sampling clock rate. This allows the desired image frequency to clock frequency ratio to be kept constant over any number of 2-to-1 downsampling stages. The sample-and-hold circuit is implemented as a fully differential switched-capacitor circuit, as shown in . The biquadratic filter used in the downsampling stages shown in . The operational amplifiers used to implement the sample-and-hold amplifier and biquadratic filter are based on the BiCMOS telescopic cascode topology shown in Figure 5. The bipolar cascoding transistors Q1 and Q2 are used to boost the unity gain bandwidth of the amplifier by providing a higher output impedance than comparable MOS transistors with the same current. Bipolar emitter followers Q3 and Q4 buffer the switching capacitance so as to minimize its effect on the settling time of the amplifier.

The prototype chip has an active area of $1.9{\times}1.9\ mm^2$ and dissipates 112 mW of power from a 3.3 V supply. The analog switched-capacitor circuits dissipate 36 mW, and the circuits used to generate the required clocks dissipate 76 mW. The large power dissipation in the clock circuits is a consequence of the large devices used to drive the clock lines with fast transition times in order to minimize clock jitter.

A plot of the measured frequency response at the output of the third downsampling stage for input signals in the range of 850-926 MHz with a 78-MHz sampling frequency is shown in Figure 6. The response of the desired channel at 884 MHz, which has a gain of 35 dB, and the frequencies that alias into this channel are identified by circles on the graph. The potential interfering channels between 850-900 MHz have been attenuated by at least 38 dB. For the narrower band from 872-884 MHz, the potential interfering channels are attenuated by at least 52 dB. The third-order intercept point of the front-end, measured with a two-tone intermodulation test, was determined to be +12 dBm. The input-referred spot noise for the system over a 30-kHz bandwidth was measured to be –80 dBm, which corresponds to a 49-dB noise figure for a 50–Ω source resistance. The kT/C noise of the switching circuits and thermal noise generated in the operational amplifiers contribute equally to the noise floor. Within the operational amplifiers, the dominant noise sources are the wideband thermal noise of the emitter followers Q3 and Q4. Because the noise has a bandwidth greater than the sampling rate, all of the noise power aliases into the 78-MHz bandwidth. The noise performance could be improved by approximately 3 dB by removing the emitter followers Q3 and Q4 and increasing the transconductance of transistors M2 and M3 in order to drive the output load. Additionally, the noise floor can be lowered by increasing the capacitor sizes in the switched-capacitor circuits. The addition of an external LNA would improve the overall noise performance by approximately 20 dB.

The authors wish to thank Texas Instruments for the fabrication of the prototype chip and T. Blalack and D. Su for their technical assistance.

*References*

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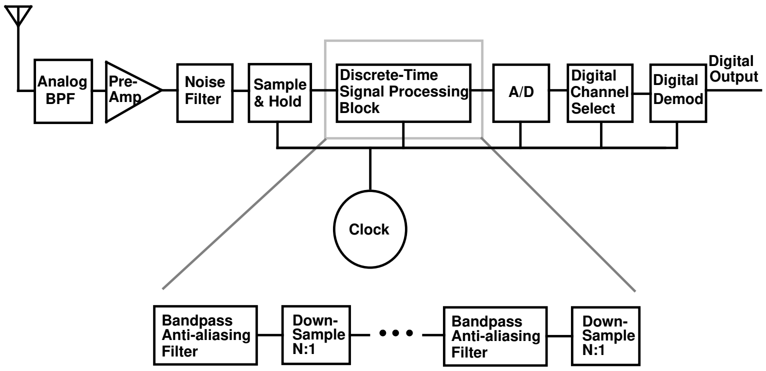


**Figure 1: Receiver Architecture.**

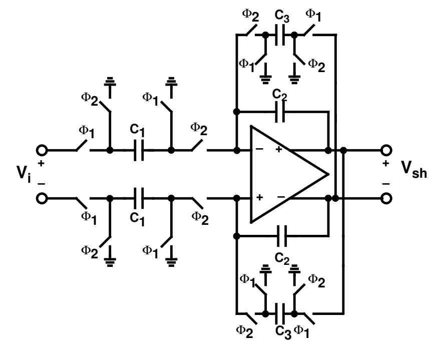


**Figure 3: Sample-and-hold circuit.**

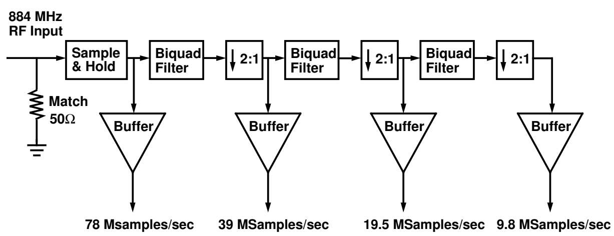


**Figure 2: Prototype chip block diagram.**

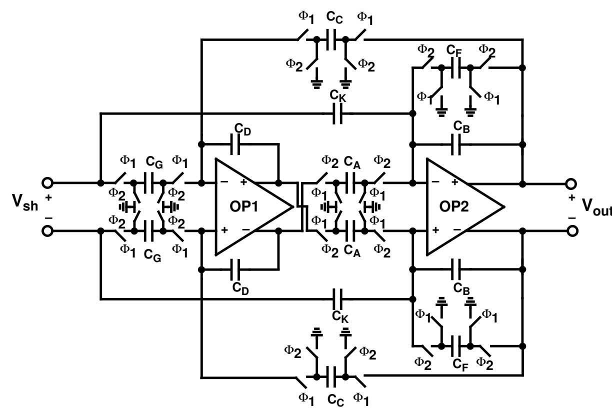


**Figure 4: Biquadratic filter circuit.**

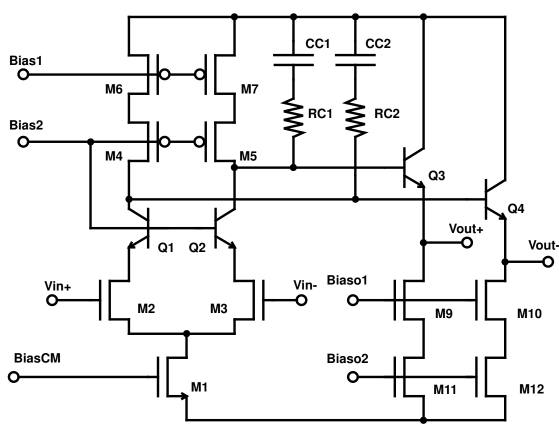


**Figure 5: Telescopic cascode amplifier.**

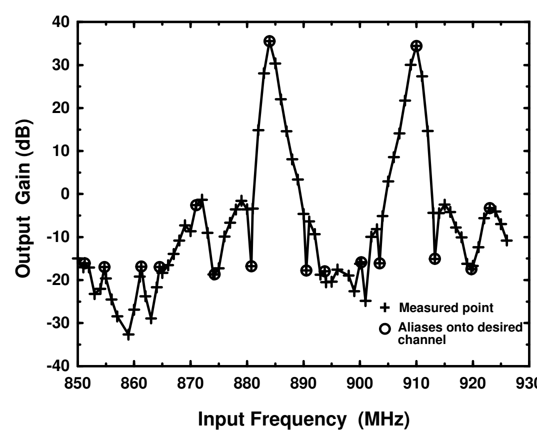


**Figure 6: Frequency response at output of third downsampling stage.**