A 15-bit Pipelined Floating-Point A/D Converter

Dwight U. Thompson
Center for Integrated Systems
Stanford University
duthomp@leland.stanford.edu

Bruce A. Wooley
Center for Integrated Systems
Stanford University
wooley@ee.stanford.edu

Abstract

A 15-bit switched-capacitor pipelined floating-point A/D converter (FADC) has been designed with a 5-bit exponent and a 10-bit mantissa. The exponent value is established by a 3-stage pipelined variable gain amplifier, while the mantissa is determined with a 10-bit uniform pipelined A/D converter. An experimental prototype of the converter has been implemented in a 0.5-μm CMOS technology. It achieves a dynamic range of 15 bits at a conversion rate of 20Msamples/sec with a total power dissipation of 380mW.

1. Introduction

The rapidly proliferating use of digital signal processing has resulted in an steadily increasing demand for higher sampling rates and lower power dissipation in high-resolution analog-to-digital converters. Application areas for high-speed, high-resolution converters include wireless communications systems, instrumentation for high-energy physics experiments, radar, and test and measurement equipment.

In recent years, switched-capacitor pipelined architectures have emerged as an especially attractive approach to implementing Nyquist-rate medium to high-resolution A/D conversion at medium to high conversion rates with relatively modest power consumption. In addition, floating-point A/D converters (FADCs) have been shown to be a useful means of providing a large dynamic range in applications where large signals need not be encoded with a precision greater than that needed for small signals. Owing to the nonuniform nature of the quantization in a floating point converter, it appears possible to sacrifice a large peak signal-to-noise ratio (SNR) to obtain savings in power dissipation and area while achieving a large dynamic range. The objective of this work is to combine the techniques of pipelining and floating-point conversion to achieve a significant increase in dynamic range without stringent linearity requirements or the overhead of complex calibration circuitry.

Floating-point analog-to-digital converters have historically been used for the instrumentation of experiments in which the acquired signal is of a non-repeatable nature, such as those resulting from explosions, impacts, or earthquakes. Specifically, they have been used for large dynamic range data acquisition in high-energy physics instrumentation, such as electromagnetic calorimeters for detectors in colliding beam machines [1]. Additionally, nonuniform converters may be attractive for wireless applications in which a low-amplitude signals must be acquired and processed with a SNR in the range of 40dB to 70dB.

The architecture described in this paper comprises a 3-stage, switched-capacitor variable gain amplifier (VGA) followed by a uniformly-quantized pipelined ADC with digital error correction. No calibration scheme is needed to achieve a peak SNDR of 60dB.

2. FADC Implementation

Floating-point A/D conversion typically consists of two operations. First, the level, or range, of the input signal magnitude is detected, and this range is encoded as an m-bit exponent. Next, the signal is quantized uniformly to obtain an n-bit mantissa. The step size with which the mantissa is quantized is scaled according to the exponent. The total resolution of the converter is n+m bits.

A block diagram of the proposed pipelined FADC architecture is shown in Figure 1. In this converter, a 3-stage, switched-capacitor variable gain amplifier is used to amplify low-level signals into the input range of the subsequent uniformly quantized pipelined A/D converter. Large amplitude signals pass directly to the pipeline A/D converter input. On-chip comparators are used to detect the input signal level and thereby determine the value of the exponent.

2.1. Variable Gain Amplifier

The input to the FADC is tracked and sampled by the first stage of the VGA. In the first two stages of the VGA the gain may be set to either unity or four, while the third stage gain is either unity or two. The larger gains are used in the first two stages of the VGA in order to minimize the sensitivity to noise in subsequent stages of the pipeline for small signals. The gain of the VGA, and thus the input signal range, is established by using two high-speed, low-offset comparators in each VGA stage to detect the signal level. The gain of each stage is established for that stage as soon as the signal level at the

stage's input is detected. Each of the three VGA stages is implemented with the topology shown in Figure 2.

The clock waveforms for the alternating odd and even numbered stages in the entire FADC pipeline, including the three VGA stages, are shown in Figure 3. These clock phases are derived from an external low-swing clock signal using an inverter chain.

During the tracking phase, when the odd-stage clock signals, Φ_{o1}, Φ_{o2}, and Φ_{o3}, are high, switches S_{in} in first and third stages of the VGA conduct, connecting the stage's input to the bottom plates of the capacitors C_s and C_f, while switches S_{cmi} and S_{cmo} connect the input and output of the op amp to their respective common-mode levels. At the end of the tracking phase, Φ_{o1} goes low and the common-mode switches, S_{cmi}, are turned off. At this point the input nodes of the op amp are floating. The delayed odd-stage clock phase Φ_{o2} then goes low and S_s turns off, effectively sampling the input voltage. Also, the level detection comparators are latched at this time. Φ_{o3} then transitions low, turning off the input switches, S_{in}, and the common-mode output switch, S_{cmo}, ending the tracking phase. Since the sampling switch turns off before the input switches, the sampling node is floating and the charge injected from the input switches does not affect the sampled value. During the time between the end of the tracking phase and the beginning of the amplify phase, the stage's two comparators that detect the input signal level are latched and thereby establish the gain of the stage during the amplify/hold phase.

The input-output transfer function for a stage in the VGA configured for non-unity gain (2 or 4) is

$$V_{out} = V_{in}\left(1 + \frac{C_s}{C_f}\right)\left(\frac{1}{1+e}\right) - \frac{V_{offset}}{f_1} \quad (1)$$

where f_1 is the feedback factor and e is the gain error:

$$f_1 = \frac{C_f}{C_s + C_f + C_{parasitic}} \quad (2)$$

$$e = \frac{1}{f(Gain_{open-loop})} \quad (3)$$

The nominal gain of the stage is simply $(1+ C_s/C_f)$. Thus, a gain of two is obtained if $C_s = C_f$, while $C_f = C_s/3$ results in a gain of four.

When configured for unity-gain, the input-output relationship for the VGA stage is

$$V_{out} = V_{in}\left(\frac{1}{1+e}\right) - \frac{V_{offset}}{f_2} \quad (4)$$

where

$$f_2 = \frac{C_s + C_f}{C_s + C_f + C_{parasitic}} \quad (5)$$

The primary differences between a VGA stage and a stage in the pipeline ADC are that no A/D conversion, D/A conversion or subtraction are needed in the VGA stage, while there is no unity-gain transfer mode in the pipeline stage, only a gain of two.

2.2. Level-Detect Comparators

The two comparators used in each VGA stage to detect the level of the input to that stage are implemented with the circuit shown in Figure 4. In this circuit, the ratio of the reference capacitors C_{ref}/C_{in} is used to establish the four desired threshold voltages of Vref/4 in the first two VGA stages and Vref/2, in the third stage. In each of the comparators, the input is first amplified by two fast, low-gain preamplifiers, and then sampled by a dynamic latch. Source followers buffer the preamp outputs from the kick-back in the dynamic latch. The low-offset comparators are precise to 11-bits. Each of the six comparators dissipates 1.3mW of static power.

2.3. Pipeline A/D Converter state

A stage of the pipelined A/D converter is shown in Figure 5. During the tracking phase it operates in the same fashion as a stage in the VGA. However, to perform the subtraction operation during the amplify/hold phase, capacitor C_f is connected to the op amp output and the capacitor C_s is connected to one of the three designated reference voltages {-Vref, 0, +Vref}. The comparator outputs determine which of the switches, S_{vp}, S_{vn}, or S_z, conduct to select the appropriate reference. If the input voltage is greater (less) than +Vref/4 (-Vref/4), then S_{vp} (S_{vn}) turns on, connecting C_s to Vref+ (Vref-). If the input voltage is between +Vref/4 and -Vref/4, then S_z connects C_s to a common-mode ground. Once the stage is appropriately configured, the residue is amplified and sampling of the residue can be performed by the next stage.

Simple, low-power dynamic comparators can be used in the pipelined A/D converter [2], since digital error correction is used to correct for the high offsets expected in such circuits. The comparators serve as a low-resolution flash A/D converter that adds little capacitance to the load on the preceding stage.

2.4. Operational Amplifiers

The operational amplifiers used in each stage of the FADC employ the telescopic cascode structure with gain boosted cascade devices shown in Figure 6 [3]. Inputs to the gain boosting amplifiers are established through the level-shifting capacitors C1-C4. Capacitive common-mode feedback, provided by capacitors C5 and C6, generates the current source bias voltage, V_{bias1}. The common mode input and output levels for both the main op amp and the gain boosting amplifiers are established during the tracking/sampling phase of each stage.

The gain boosting amplifiers are also telescopic cascode circuits with capacitive common mode feedback. The tele-

scopic cascode topology provides a high-speed, single-stage design with minimal power dissipation. The open-loop gain of each of the main telescopic op amps is estimated to be at least 110dB.

3. Experimental Results

An experimental 15-bit FADC was designed and implemented in a 0.5-µm, triple metal, CMOS technology with linear poly/N-well capacitors. The static power dissipation was measured at 122mW at 5V supply and 4.5V digital supply. The die photo of the pad-limited design, 4.3mm x 3.2mm, is shown in Figure 7.

To minimize offsets and capacitor mismatch, special care was taken in the physical layout of the converter [4]. Precautions taken include shielding sensitive signal locations, common-centroid device placement, and separation of the analog and digital circuitry. Separate supplies were used for the clock generator, output drivers, as well as for the analog and digital sections. As a result of the care taken in the layout, no calibration is need to achieve a linearity of 10 bits.

A plot of the signal-to-noise+distortion (SNDR) of the experimental FADC as a function of the input signal level shown in Figure 8. The peak SNDR for the converter is 60dB and the maximum dynamic range is 90dB for an input sinusoid of 2.14MHz sampled at a rate of 20MSample/s. Figure 9 is a FFT plot of the spectrum of the converter at an input frequency of 9.33MHz.

The measured performance of the experimental FADC is summarized in Table 1.

4. Conclusion

Floating-point A/D conversion enables the digitization of analog signals with an extended dynamic range. This conversion technique can reduce the need for calibration and high linearity while still achieving a large dynamic range. An experimental prototype has demonstrated the successful operation of this type of converter with a 10-bit mantissa and a 5-bit exponent at a sampling rate of 20MSamples/s.

5. References

[1] G. M. Haller, and D. R. Freytag, "Analog Floating-Point BiCMOS Sampling Chip and Architecture of the *BaBar* CsI Calorimeter Front-End Electronics System at the SLAC B-Factory," *IEEE Trans. Nuc. Sci.*, vol. 43, pp. 1610-1614, June 1996, pt. 2.

[2] T. B. Cho, and P. R. Gray, "A 10 b, 20 Msamples/s, 35mW Pipeline A/D Converter," *IEEE JSSC*, vol. 30, pp. 166-172, Mar. 1995.

[3] J. M. Ingino, and B. A. Wooley, "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter," *IEEE JSSC*, vol. 33, pp. 1920-1931, Dec. 1998.

[4] M. J. McNutt, S. LeMarquis, and J. L. Dunkley, "Systematic Capacitance Matching Errors and Corrective Layout Procedures," *IEEE JSSC*, vol. 29, pp. 611-616, May 1994.

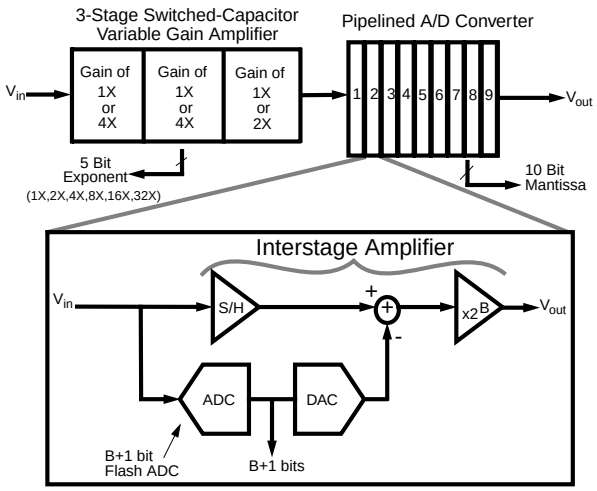

Figure 1. Floating-point A/D converter architecture

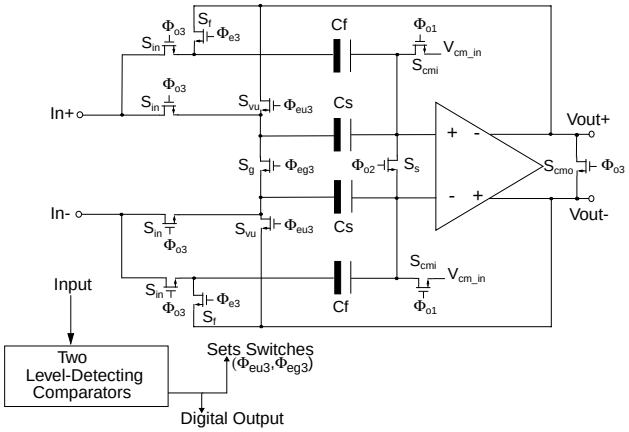

Figure 2. Stage of variable gain amplifier

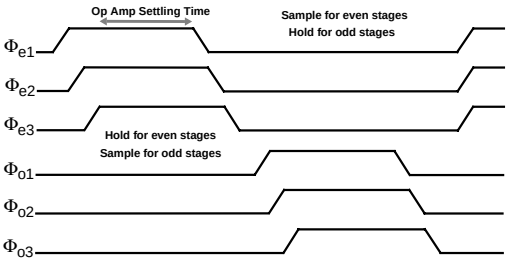

Figure 3. Clock waveforms

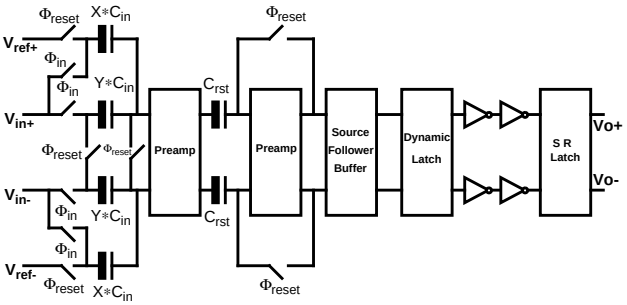

Figure 4. Comparator with offset cancellation

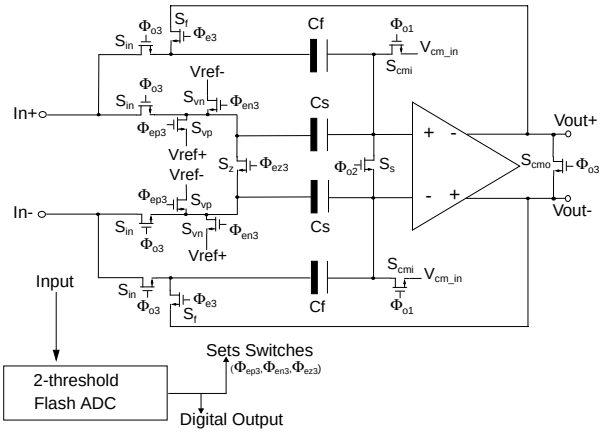

Figure 5. Stage of pipelined A/D converter

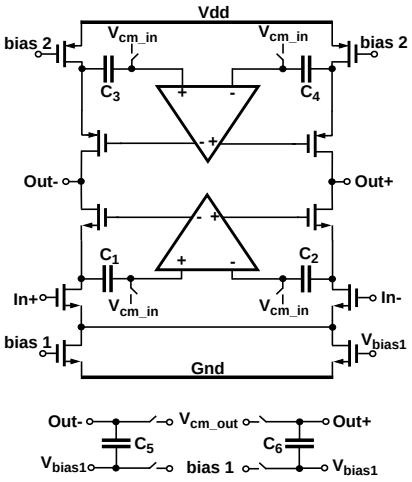

Figure 6. Op amp with common mode feedback

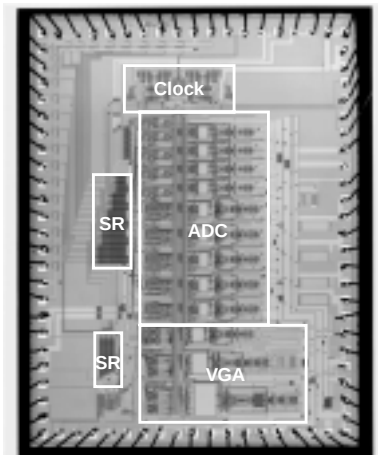

Figure 7. Die photo

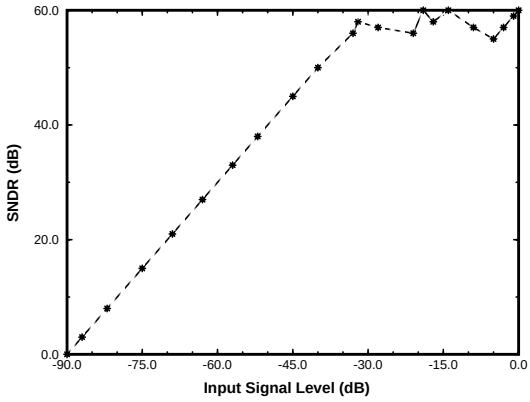

Figure 8. Measured SNDR versus input signal level

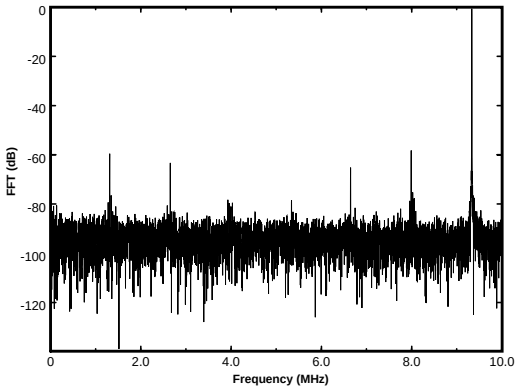

Figure 9. FFT spectrum of FADC at 9.33MHz

Table 1: Performance Summary

Parameter	Value
Sampling Speed	20MHz
Peak SNR/SNDR	60dB
Peak Dynamic Range	90dB
Supply Voltage	5V (analog), 4.5V (digital)
Total Power dissipation	380mW
Static Power dissipation	122mW
Technology	0.5-μm single-poly, tri-metal CMOS with linear poly/N-well capacitors
Active Area	4.3mm x 3.2mm