BANDPASS ANALOG-TO-DIGITAL CONVERSION FOR WIRELESS APPLICATIONS

by

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Abstract

Oversampled bandpass A/D converters based on sigma-delta (ΣΔ) modulation can be used to robustly digitize the narrowband intermediate frequency (IF) signals that arise in radios and cellular systems. Digitization of the IF processing confers several important advantages in a receiver, including greater reliability, potentially lower power dissipation, and improved performance as technology scales. Moreover, by converting to digital at the IF location, the problems of low frequency ($1/f$) noise and dc offset are avoided.

The implementation of a high-speed bandpass ΣΔ modulator that achieves the large dynamic range needed for narrowband wireless-channel digitization involves significant challenges that are explored in this research. This dissertation describes a new two-path architecture for a fourth-order, bandpass ΣΔ modulator that is more tolerant of analog circuit limitations at high sampling speeds than conventional implementations based on the use of switched-capacitor biquadratic filters. Nonideal effects relating to this new two-path architecture, such as timing jitter, path mismatch, and potential instability are described and analyzed. An experimental prototype employing the two-path topology has been integrated in a 0.6-μm, single-poly, triple-metal CMOS technology with capacitors synthesized from a stacked-metal structure. Two interleaved paths clocked at 40 MHz digitize a 200-kHz bandwidth signal centered at 20 MHz with 75 dB of dynamic range while

suppressing the undesired mirror image signal by 42 dB. At low input signal levels, the mixing of spurious tones at dc and $f_s/2$ with the input appears to degrade the performance of the modulator; out-of-band sinusoidal dither is shown to be an effective means of avoiding this degradation. The experimental modulator dissipates 72 mW from a 3.3-V supply.

An analysis of noise in the experimental prototype reveals that its inband noise floor is dominated by a combination of amplifier noise and thermal noise from switches. The measured dynamic range of the experimental prototype lies within 2 dB of that predicted by hand analysis.

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I wish to acknowledge the many people who have assisted me in this work and made my experience at Stanford so enjoyable. First and foremost, I thank Professor Bruce Wooley for having accepted me into his research group when I was capable of little, except to articulate my desire to do research in electronic circuit design. He has given me excellent guidance throughout the years and has instilled in me an appreciation for communicating clearly. He impresses me as someone who combines an uncommon ear for language with the rare ability to elicit clarity from the writing of students through his bold editing. Any obfuscation in this thesis is reflective solely of my own inadequacy. In the future, I will strive to apply the same exacting standards to myself as Professor Wooley has to me.

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Chapter 1 *Introduction*

The role and infrastructure of wireless communications have grown dramatically since the initial deployment of the cellular mobile telephone system in the 1980s. From its modest beginnings characterized by a low subscriber base with telephones having radio transceivers only slightly more sophisticated than two-way FM radios, global cellular radio systems now encompass over 150 million subscribers and enable new paradigms of access including paging, facsimile, and data services, in addition to voice. The impressive rate of growth in both subscriber base and technological innovation will remain unchecked as latent markets in the Asia/Pacific region and the Indian subcontinent emerge. It has been predicted that there will be 350 million users of mobile communications worldwide by 2005. Tables 1.1(a) and (b) summarize the top ten cellular markets in terms of subscribers and penetration in 1997 [1].

1.1 Motivation

First-generation analog cellular systems such as Advanced Mobile Phone System (AMPS) in the United States, Nordic Mobile Telephone (NMT) in the Scandinavian countries, and Total Access Communication System (TACS) in the United Kingdom were only intended for speech communication. Therefore, the early standards could not accommodate mobile users who demanded value-added services such as paging and short messaging functions. In addition, the early standards were marked by their incompatibility, thus restricting mobile users to the area served by their network provider. These limitations stimulated the development of second-generation, unified, cellular standards that embraced a robust data-carrying capacity as well.

Country	Subscribers
United States	55,312,300
Japan	38,253,900
China	13,233,000
Italy	11,737,900
Germany	8,170,000
United Kingdom	7,109,400
South Korea	6,910,000
France	5,817,300
Australia	4,893,000
Brazil	4,400,000

(a)

Country	Penetration (per 100 pop.)
Finland	41.98
Norway	38.07
Sweden	35.82
Hong Kong	34.29
Japan	30.3
Israel	28.32
Denmark	27.49
Australia	26.32
Iceland	24.20
Singapore	22.55

(b)

Table 1.1: Top ten cellular markets in terms of (a) subscribers, and (b) penetration per 100 population in 1997.

The pan-European Global Standard of Mobile communications (GSM) was proposed in 1985, and the first GSM networks were deployed in 1991. Simultaneously in the United States, several competing standards have been proposed and are currently being implemented. The North American standards include a time-division multiple access scheme, IS-54 (D-AMPS), and a spread spectrum code division multiple access protocol, IS-95 (CDMA). In the future, both the European and North American digital cellular standards will continue to evolve and an increasing amount of functionality will be incorporated into the mobile terminal. Potential new services include remote database access, wireless email, video on demand, and global positioning.

The fragmentation in both first- and second-generation cellular standards raises a myriad of distressing concerns for network providers, system designers, circuit engineers, and consumers alike. Moreover, this lack of unity has stymied the rapid adoption of each subsequent generation of cellular technology by the consumer, who is faced with

differentiating between multiple and competing standards, each promising services yet to be delivered. As a means of meeting this challenge, engineering effort is now being devoted to the development of integrated radio receiver platforms that support multiple standards. Until the market rallies behind a universally accepted standard, dual- or even multi-mode radios and mobile units will be needed to provide seamless coverage across service boundaries. As an example, one already sees dual analog/digital handsets in the market as North American cellular subscribers transition from AMPS to IS-54 or IS-95.

Particular engineering attention is directed towards reducing power dissipation and ensuring flexibility in wireless receiver architectures. By increasing the level of integration in the signal path, a receiver can be realized with a more compact form factor at reduced cost and with greater reliability. In addition, higher levels of integration reduce the need for the constituent analog and mixed-signal circuit blocks to drive large pad and package parasitic capacitances, thereby conserving power. Aggressive utilization of VLSI technology also enables the combined integration of a bandpass or baseband analog-to-digital (A/D) converter along with the traditional front-end receiver building blocks. In this manner, the back-end signal processing can be shifted from the analog domain into the digital domain. Digitization in the signal path of the receiver, whether at an intermediate frequency, or at baseband, is rapidly becoming a necessity because emerging digital cellular standards encompass bandwidth-efficient modulation schemes, as well as compression, error correction, and multipath equalization or spread spectrum techniques, that require substantial digital processing [2], [3].

To meet the anticipated requirements imposed by digital cellular standards, the next generation of portable, agile, and programmable radio receivers is evolving towards an integrated digital solution in which the RF is translated down to a low intermediate frequency (IF) or to baseband before being digitized and processed. In this type of architecture, the processor can control narrowband channel characteristics such as bandwidth and the rejection of adjacent interferers by means of numerical parameters. Also, the radio will be able to dynamically adapt as the characteristics of the wireless channel itself change as a function of time. These advantages open the possibility of implementing

software-controlled radios that can support multiple standards and are suitable for use in widely varying propagation environments.

This research studies the challenges involved in implementing bandpass A/D conversion in the receiver signal path. In this approach, the baseband signal processing is moved into the digital domain where the quality of the demodulation is not compromised by noise or other analog imperfections. Bandpass sigma-delta (ΣΔ) modulation is studied as the method of choice for implementing high-frequency, narrowband A/D conversion. This dissertation proposes a two-path architecture for a fourth-order, bandpass ΣΔ modulator that is more tolerant of analog circuit limitations at high sampling speeds than conventional implementations based on the use of switched-capacitor biquadratic filters. An experimental prototype employing the two-path topology has been integrated in a 0.6-μm, single-poly, triple-metal CMOS technology with capacitors synthesized from a stacked-metal structure. Two interleaved paths clocked at 40 MHz digitize a 200-kHz bandwidth signal centered at 20 MHz with 75 dB of dynamic range while suppressing the undesired mirror image signal by 42 dB. At low input signal levels, the mixing of spurious tones at dc and $f_s/2$ with the input appears to degrade the performance of the modulator; out-of-band sinusoidal dither is shown to be an effective means of avoiding this degradation. The experimental modulator dissipates 72 mW from a 3.3-V supply.

1.2 Organization

This dissertation is organized into eight chapters, including this introduction. The next chapter briefly reviews the superheterodyne receiver architecture. Various methods for demodulating and digitizing the signal at the back end of a superheterodyne receiver are examined. Errors associated with the separation of the desired signal into its inphase (I) and quadrature (Q) components are discussed, and bandpass analog-to-digital conversion is introduced as an approach that is especially amenable to channel filtering and I/Q extraction in the digital domain. Chapter 3 is devoted to an overview of both lowpass and bandpass analog-to-digital conversion using sigma-delta (ΣΔ) modulation. Chapter 4 dis-

cusses the system-level design and analog circuit requirements for a fourth-order, $f_s/4$ modulator that digitizes a signal passband centered as high as 20 MHz. The performance impairments of bandpass modulators operating at high sampling rates are identified, and an *N*-path modulator architecture is proposed in Chapter 5 as an effective means to implement a high-speed bandpass modulator. The design of the experimental modulator is presented in Chapter 6, followed by a description of the test setup and a discussion of the measured results in Chapter 7. Tones in the noise spectrum are shown to cause substantial degradation at low input signal levels, and dithering is identified as a solution to this problem in the experimental modulator. A summary of the results, as well as suggestions for further exploration, complete this dissertation in Chapter 8.

Chapter

2

IF Processing in Radio Receivers

The purpose of a radio frequency (RF) receiver is to extract a desired signal in the presence of noise and interfering signals that coexist with that signal in the electromagnetic spectrum. At the antenna, the power of the desired signal may be on the order of –110 dBm (0.71 μV_{rms} in a 50-Ω system), while interfering signals in adjacent and alternate channels may have power levels that are 30-60 dB higher. Following detection, a receiver must amplify the signal, suppress interferers and extract the modulated information. The receiver's performance is measured by its sensitivity, which refers to its ability to detect signals in the absence of any interference other than thermal noise, and its selectivity, which measures its ability to discriminate between the desired signal and large adjacent-channel interferers. Typically, a receiver's sensitivity is determined by the noise performance of its front-end circuitry, while selectivity is determined by filtering after the RF signal has been mixed to an intermediate frequency (IF) or to baseband. This chapter is primarily concerned with selectivity and integration issues at a receiver's back-end, which encompasses the IF and baseband circuitry.

This chapter begins with a brief review of superheterodyne receivers, the most widely used receiver architecture. Then several methods for demodulating and digitizing the signal at the back-end of a superheterodyne receiver are examined. Errors associated with the separation of the signal into its inphase (I) and quadrature (Q) components are analyzed, and bandpass analog-to-digital conversion is proposed as an approach that is especially amenable to IF digitization with subsequent I/Q extraction and channel-select filtering in the digital domain.

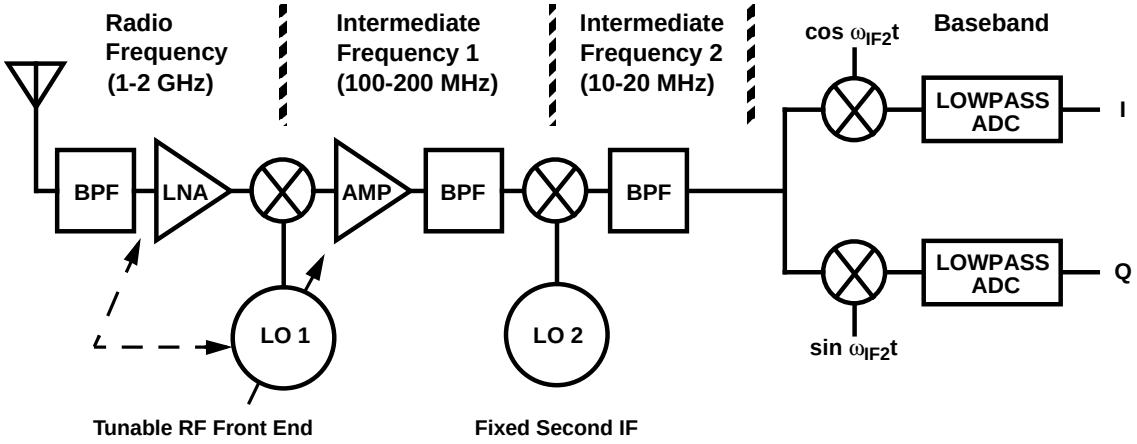


Figure 2.1: Dual-IF, superheterodyne receiver architecture with baseband A/D conversion.

2.1 Superheterodyne Receiver Architecture

A block diagram of a double-conversion, or dual-IF, superheterodyne receiver is shown in Figure 2.1 [72]. The receiver is comprised of a tunable front-end bandpass filter, a low-noise amplifier (LNA), which reduces the input-referred noise contributions of subsequent stages in the receiver, and two stages of mixing, intermediate frequency filtering and amplification. At the second IF, the signal is multiplied by two carriers that are 90° out of phase in order to demodulate the signal into its *I* and *Q* components, which are then digitized at baseband by two parallel lowpass A/D converters. The use of two intermediate frequencies distinguishes dual-IF architectures from those that employ a single IF, or in some cases, more than two IF stages. The principles of operation among these architectures is similar; the use of more than one IF stage merely allows for more manageable tradeoffs between receiver selectivity and image rejection at the cost of greater complexity and increased power dissipation. These issues are reviewed in more detail in [4], and a case study that examines system-level noise and distortion requirements in a superheterodyne receiver for an IS-55 [5], dual-mode, digital cellular telephone can be found in [6].

2.1.1 Frequency Downconversion

In Figure 2.1, the incoming signal at the antenna is first selected and amplified by the receiver's front-end, which is tuned to the RF carrier frequency. With a typical carrier frequency in the GHz range, the front-end bandpass filter has a relatively broad bandwidth of tens of MHz. This filter, which selects the RF band of interest, thus passes the desired signal together with any adjacent-channel and nearby interferers that might be present. The front-end filter also performs image-reject filtering prior to the frequency translation down to the first IF. Image-reject filtering must precede any downconversion operation to an intermediate frequency. As illustrated in Figure 2.2, if the desired signal is centered at f_{RF}, then image-band signals centered at $f_{RF} - 2 \times f_{IF}$ must be filtered out prior to mixing. Otherwise, they can corrupt the desired signal by downconverting into the same intermediate frequency, f_{IF}. Typical receiver requirements for image rejection range from 40 to 90 dB [7].

In a dual-IF architecture, the choice of first and second intermediate frequencies is governed by a tradeoff between filter selectivity and image rejection. As shown in Figure 2.2, the image-reject filter must attenuate signals in the image band located only $2 \times f_{IF}$ away from the desired signal. The two requirements imposed upon an image-reject filter, (1) a well-controlled response in the signal passband and (2) a steep attenuation in the image band, can be met simultaneously if $2 \times f_{IF}$ is sufficiently large. However, f_{IF} should not be too large if the basic principle underlying the need for frequency downconversion, which is to translate the RF signal down to a frequency where channel-select filtering becomes practical, is to be met. As a rough rule-of-thumb for implementation reasons, the relative bandwidth of the image-reject filter, which is the ratio of the filter's passband bandwidth, B, to its passband center frequency, f_c, should be kept within the range [72]

$$0.01 < \frac{B}{f_c} < 0.1 \quad . \tag{2.1}$$

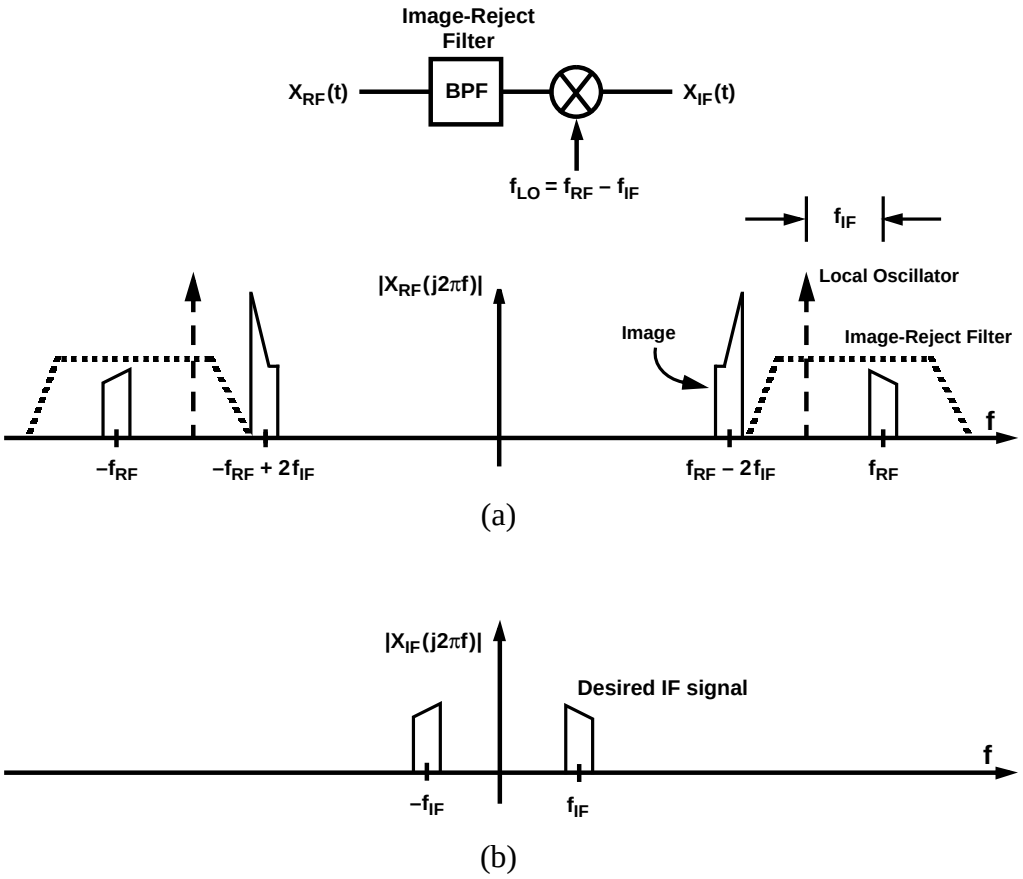


Figure 2.2: (a) The spectrum of $x_{RF}(t)$, prior to filtering and mixing, which shows an undesired signal in the image band, and (b) the spectrum of the intermediate frequency signal, $x_{IF}(t)$, following filtering and mixing.

This implies, for example, that the ratio of the carrier frequency to the intermediate frequency might be approximately 10 to 1. Therefore, when the carrier of the incoming RF signal is situated between 1 and 2 GHz, a first IF between 100 and 200 MHz and a second IF between 10 and 20 MHz are typical choices.

2.1.2 Channel-Select Filtering

In dual-IF, superheterodyne receivers, selectivity is typically concentrated in the intermediate frequency filters. High-selectivity, fixed-frequency, second-IF filters [72] implemented with discrete components suppress interfering signals in adjacent and alternate channels. The desired channel is then mixed to baseband for A/D conversion and digital processing as depicted in Figure 2.1. The IF filters often include crystal or dielectric resonators that cannot be integrated in a monolithic circuit. Therefore, a conventional superheterodyne back-end architecture, in which channel-select filtering is performed prior to baseband processing, is not readily amenable to a fully-integrated implementation.

A low-IF, superheterodyne receiver topology has been proposed as a means of enabling the monolithic integration of the channel-select filters [89]. The premise of this approach is that with a sufficiently low IF (< 1 MHz), the channel-select filters can be implemented using established integrated circuit filtering techniques such as those based on g_m-C or switched-capacitor topologies. However, the use of a low IF reintroduces the problem of suppressing signals in the image band when the RF signal is mixed down to the low intermediate frequency. Since the relative bandwidth of an image-reject filter for low-IF receivers is likely to be prohibitively small, an image-reject mixer [7] is typically employed to mix the RF signal down to IF.

One example of an image-reject mixer is shown in Figure 2.3. The RF signal, $x_{RF}(t)$, is multiplied by quadrature carriers, $\sin(\omega_{LO}t)$ and $\cos(\omega_{LO}t)$, where $f_{LO} = f_{RF} - f_{IF}$. Following the mixing operation, lowpass filtering removes the sum-frequency terms in both mixer paths. Of the remaining difference-frequency terms, the desired signals are equivalent in both paths, but the image-band signals are in quadrature. Thus, the addition of a 90° phase shifter in one path allows for the cancellation of image-band signals when the outputs of the two paths are summed together. Consequently, it is not necessary to filter the RF signal prior to image-reject mixing. In practice, however, errors in the quadrature local oscillators, as well as gain and phase mismatches in the two paths of an image-reject mixer, limit the degree of image rejection that can be achieved. A full analysis of the mixer

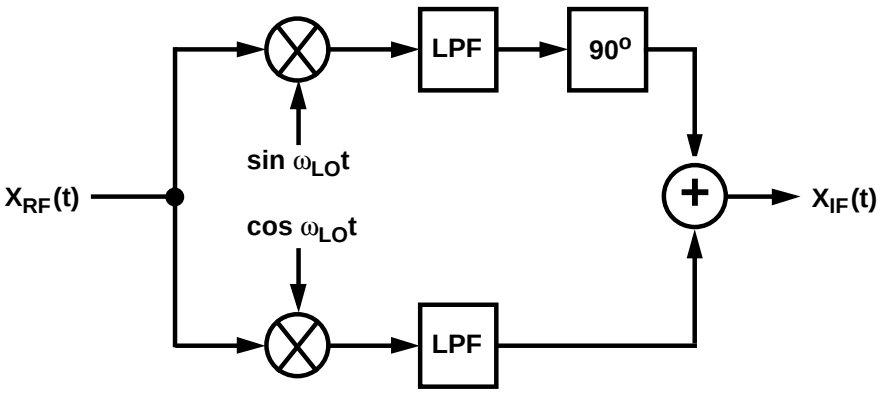


Figure 2.3: Hartley image-reject mixer.

topology in Figure 2.3 shows that a 1° phase error in the quadrature LOs and a 0.1% gain mismatch between the two mixer paths corresponds to approximately 40 dB of image rejection [7]. Since receivers typically require 40-90 dB of image suppression, some filtering is still necessary prior to image-reject mixing, and the difficulty of integrating such filters remains an issue.

This dissertation explores the premise that in order to fully integrate the back-end of a superheterodyne receiver, it is necessary to digitize the received signal prior to channel-select filtering. The received signal can be digitized at an intermediate frequency or at baseband, following analog *I* and *Q* demodulation. However, in both cases, because the channel is to be digitally selected, the dynamic range of the A/D converter, or converters, must be large enough to avoid saturation in the presence of high-power interferers that are digitized along with the desired signal. Since interfering signals can be 30-60 dB larger than the desired signal, A/D converters intended for wireless-channel digitization must usually have a dynamic range of 70 dB or more. This ensures that the desired channel is digitized with a signal-to-noise ratio of at least 10 dB, which is typically sufficient to guarantee a low bit error rate upon demodulation for many wireless standards. A/D converters based on lowpass sigma-delta modulation have demonstrated the dynamic range needed for baseband digitization of wireless channels. However, high power dissipation remains

an issue in the prototypes reported to date. In one example, a lowpass ΣΔ modulator with a 2-2-2 cascade architecture has been integrated in a 0.72-μm CMOS technology [15]. This prototype has demonstrated 71 dB of peak SNDR and 77 dB of dynamic range in a 700-kHz bandwidth with 81 mW of power dissipation from a 3.3-V supply. Thus, with two such A/D converters used in the superheterodyne receiver topology depicted in Figure 2.1, it appears feasible to perform channel-select filtering in the digital domain if the desired signal has a bandwidth as high as several hundred kHz. Sections 2.2 and 2.3 describe two alternative approaches, interleaved IF subsampling and IF digitization, that can also be used to integrate the back-end circuitry for a superheterodyne receiver. IF digitization is proposed as the method of choice since this technique allows for digital channel selection and is not susceptible to errors introduced by imperfect analog *I* and *Q* demodulation.

2.1.3 Analog *I*/*Q* Demodulation

At the second-IF location in the superheterodyne architecture of Figure 2.1, the received signal is multiplied by two carriers that are 90° out of phase in order to separate the signal into its inphase and quadrature components, $x_I(t)$ and $x_Q(t)$, respectively. In Figure 2.1, immediately after mixing to the second IF, the received signal, $x_{IF2}(t)$, can be written in terms of its inphase and quadrature components as

$$x_{IF2}(t) = x_I(t)\cos\omega_{IF2}t + x_Q(t)\sin\omega_{IF2}t \quad . \tag{2.2}$$

Thus, the baseband inphase component, $x_I(t)$, can be recovered by multiplying $x_{IF2}(t)$ by $\cos(\omega_{IF2}t)$ and lowpass filtering the result to remove the sum-frequency terms that result from the multiplication. Similarly, the baseband quadrature component, $x_Q(t)$, can be recovered by multiplying $x_{IF2}(t)$ by $\sin(\omega_{IF2}t)$ and filtering out the sum-frequency terms.

If there is a phase error in the local oscillators or a gain mismatch between the two mixer paths, then the quality of the baseband signal is degraded because of leakage between the nominally independent inphase and quadrature signal components. Consider a deviation from quadrature by ϕ radians ($\phi << \pi/2$) in the two local oscillators depicted in

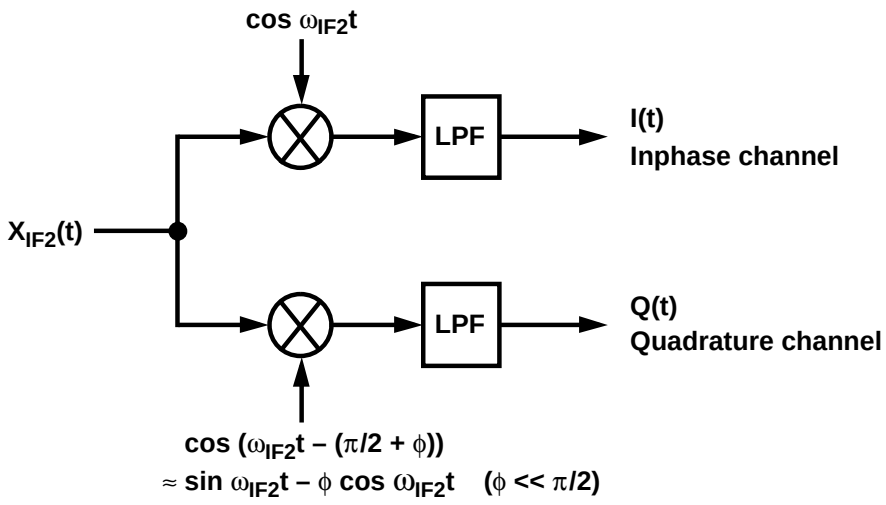


Figure 2.4: Analog *I*/*Q* demodulation with a phase error, ϕ, in the quadrature local oscillators.

Figure 2.4. The degradation in the baseband signal caused by this LO phase error can be quantified as follows. If the desired signal at f_{IF2}, is a single sinusoid

$$x_{IF2}(t) = A\cos(\omega_{IF2} + \omega_x)t \tag{2.3}$$

where $\omega_x << \omega_{IF2}$, then the output of the inphase channel is

$$I(t) = \frac{A}{2}\cos\omega_x t \quad . \tag{2.4}$$

In (2.4) it has been assumed that a lowpass filter eliminates the sum-frequency term that results from the mixing operation. With a phase variation, ϕ, from quadrature in the local oscillators, the output of the quadrature channel is

$$Q(t) = -\frac{A}{2}\sin\omega_x t - \phi\frac{A}{2}\cos\omega_x t \quad . \tag{2.5}$$

The complex baseband signal, $x_b(t)$, is then

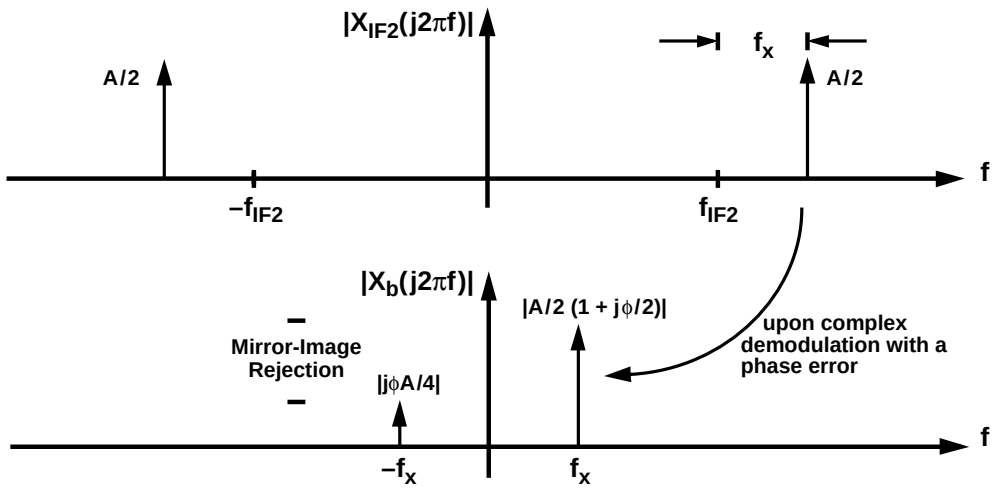


Figure 2.5: Frequency spectrum of $x_b(t)$ after analog I/Q demodulation with a phase error, ϕ, between carriers nominally in quadrature.

$$\begin{aligned} x_b(t) &= I(t) - jQ(t) \\ &= \frac{A}{2}(\cos\omega_x t + j\sin\omega_x t) + j\phi\frac{A}{2}\cos\omega_x t \\ &= \frac{A}{2}e^{j\omega_x t} + j\phi\frac{A}{2}\cos\omega_x t \quad . \end{aligned} \tag{2.6}$$

This result indicates that $x_b(t)$ comprises the desired signal, which is a single tone at frequency ω_x, together with an error term that contains spectral components at ω_x and the mirror frequency, $-\omega_x$, as illustrated in Figure 2.5. Thus, a phase error between the two LOs in Figure 2.4 results in a mirror signal, also called mirror image, that is a scaled replica of the desired signal. The degree of mirror-image rejection, *IR*, is defined as the ratio of the power of the mirror tone at $-\omega_x$ to the power of the desired tone at ω_x and is equal to

$$IR = \frac{P_{im}}{P_{des}} = \frac{\left| j\phi\frac{A}{4} \right|^2}{\left| \frac{A}{2}\left(1 + j\frac{\phi}{2}\right) \right|^2} = \frac{\phi^2}{4(1 + \phi^2/4)} \tag{2.7}$$

$$\approx \frac{\phi^2}{4} \ , \quad \phi << 1 \ .$$

Without special trimming or analog tuning techniques, it is difficult to reduce the phase error between the LO signals significantly below 1° [91]. Therefore, assuming a phase error of 1°, the unwanted mirror image will be suppressed by approximately 40 dB.

A similar analysis that accounts for amplitude imbalance in the local oscillators can be carried out to yield

$$IR = \frac{(\Delta A/A)^2}{4} \tag{2.8}$$

where $\Delta A/A$ denotes the relative amplitude difference between the two local oscillator signals with nominally equal amplitudes [4].

In the preceding analyses, it is important to recognize that the mirror-image signals introduced by gain and phase imbalance in the analog I/Q demodulation process are qualitatively different from the image-band signals depicted in Figure 2.2 that mix into the same intermediate frequency as the desired signal upon downconversion. Mirror signals at baseband owing to imperfect I/Q demodulation are merely scaled replicas of the desired signal; they are guaranteed to be suppressed by an amount that depends on the mismatch between the I and Q paths, and only 25 dB of mirror-image suppression is considered adequate for many applications [89]. In contrast, signals in the image band that lie $2 \times f_{IF}$ away from the desired signal are unrelated to and can be 30-60 dB larger than the desired signal. In order to guarantee that the desired signal is at least 25 dB larger than any signals in the image band, image-reject filters must attenuate these signals by almost 90 dB.

In the remainder of this thesis, care is taken to distinguish between mirror signals (also called mirror-image signals) and image-band signals. In particular, it is emphasized that

mirror signals are always scaled replicas of desired signals that typically arise as a result of circuit mismatches or local oscillator gain and phase imbalances. Signals in the image band, however, exist independently of the desired signal and can be much larger in power. In this work, it is assumed that image-band signals are attenuated prior to any frequency translation from RF to IF, as depicted in Figure 2.2. This does not preclude the possibility of mirror signals arising from nonidealities in a receiver's back-end circuitry. In the preceding discussion, imperfect analog I/Q demodulation is shown to be one means by which a mirror image is generated in the output spectrum of a demodulated signal. An important and analogous effect, which will be discussed in detail in Chapter 5, results from path mismatch in an N-path filter.

2.2 Interleaved IF Subsampling

One proposal for reducing the sensitivity of the I/Q demodulation process in a superheterodyne receiver to analog circuit imperfections involves replacing the analog mixers in the inphase and quadrature branches with a pair of A/D converters that subsample the IF signal [8]. In effect, subsampling the IF signal performs an equivalent mixing of the signal down to baseband. A block diagram of a dual-IF receiver with an interleaved subsampling back-end is depicted in Figure 2.6. This receiver's back-end is comprised of two interleaved, lowpass A/D converters that subsample the second-IF signal, $x_{IF2}(t)$, at a rate equal to its carrier frequency, f_{IF2}. Although the sampling frequency is less than twice the highest frequency component in $x_{IF2}(t)$, destructive aliasing is avoided because f_{IF2} is presumed to be much higher than the bandwidth of $x_{IF2}(t)$ [59].

If the bandpass signal, $x_{IF2}(t)$, is written in the following general form

$$x_{IF2}(t) = x_I(t)\cos\omega_{IF2}t + x_Q(t)\sin\omega_{IF2}t \ , \tag{2.9}$$

then upon sampling at $f_s = 1/T_s = \omega_{IF2}/2\pi$, the inphase signal, $I(t)$, is

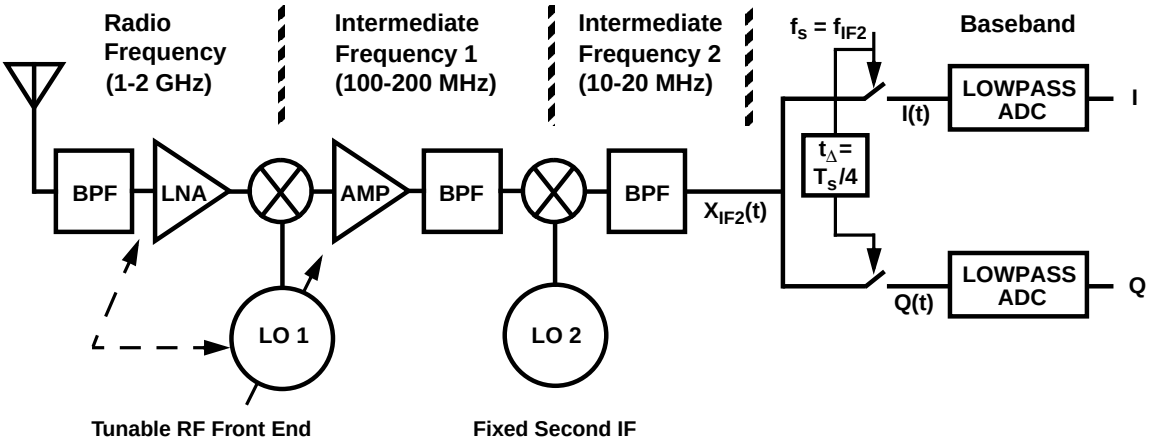


Figure 2.6: Superheterodyne receiver with an interleaved sampling *I*/*Q* demodulator.

$$\begin{aligned} I(t) &= x_{IF2}(nT_s) \\ &= x_I(nT_s)\cos\omega_{IF2}nT_s + x_Q(nT_s)\sin\omega_{IF2}nT_s \\ &= x_I(nT_s)\cos 2\pi n + x_Q(nT_s)\sin 2\pi n \\ &= x_I(nT_s)\ . \end{aligned} \tag{2.10}$$

Similarly, the quadrature signal, $Q(t)$, is

$$Q(t) = x_{IF2}(nT_s + T_s/4) = x_Q(nT_s + T_s/4)\ . \tag{2.11}$$

(2.10) and (2.11) indicate that the inphase signal, $x_I(t)$, can be recovered exactly, while there is an error in the recovery of the quadrature signal, $x_Q(t)$, that originates from the deliberate skew, $t_\Delta = T_s/4$, introduced between the sampling instances in the *I* and *Q* paths. It is claimed that in applications where the sampling frequency, f_s, is high relative to the bandwidth of the baseband signals, $x_I(t)$ and $x_Q(t)$, the error owing to systematic timing skew, $e_{skew}(nT_s)$,

$$e_{skew}(nT_s) = x_Q(nT_s + T_s/4) - x_Q(nT_s)\ , \tag{2.12}$$

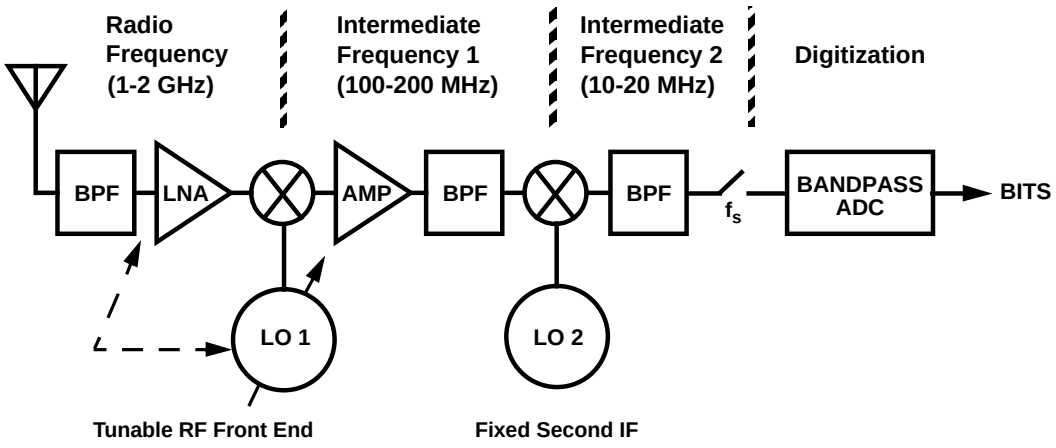


Figure 2.7: Superheterodyne receiver incorporating IF digitization via bandpass A/D conversion.

is negligible [8].

By employing an interleaved subsampling I/Q demodulator, one set of analog mixers at the back-end of a superheterodyne receiver can be eliminated, but at the expense of operating the A/D converters in the I and Q channels at higher sampling speeds. The resulting increase in power dissipation may be of concern. Furthermore, if the delay between the sampling clocks, t_Δ, differs slightly from $T_s/4$ by an amount e_Δ, then there will be a leakage signal between the I and Q channels with a power proportional to e_Δ^2. This leakage results in an incomplete mirror-image suppression that is analogous to mirror-image signals arising from phase and amplitude errors in analog I/Q demodulation.

2.3 IF Digitization

Many of the errors arising from nonideal analog circuitry in the back-end of a superheterodyne receiver can be avoided by digitizing the signal at an intermediate frequency rather than at baseband. In the IF sampling architecture depicted in Figure 2.7, the RF signal enters at the antenna and is mixed through two stages and broadly filtered before being digitized at the second-IF location by a bandpass A/D converter.

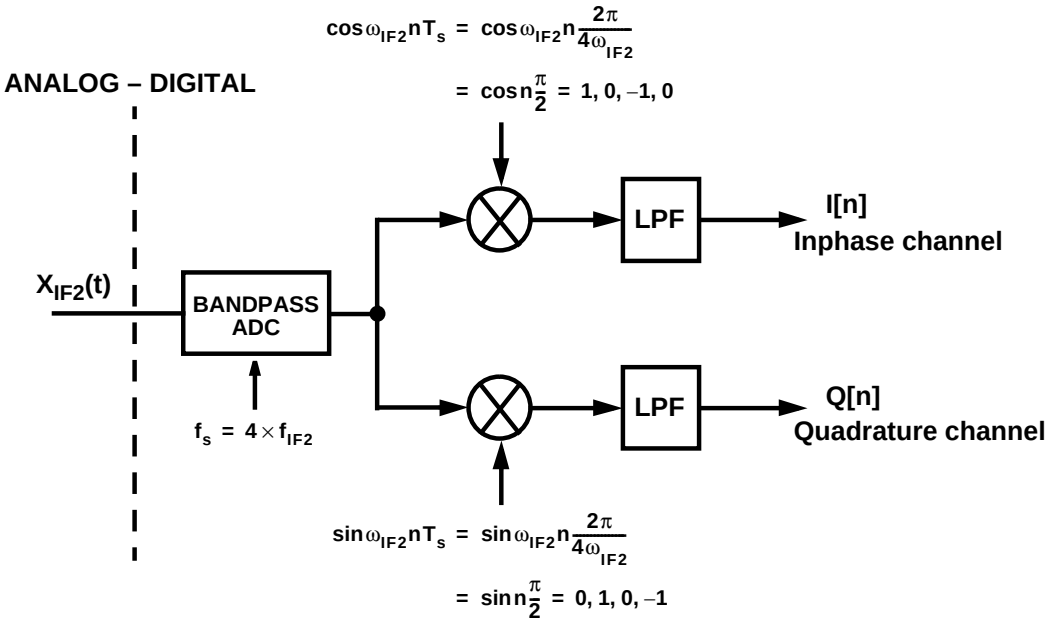


Figure 2.8: Digital I/Q demodulation of a signal centered at $f_s/4$.

IF digitization confers several advantages. First, the I and Q components of the signal are separated in the digital domain rather than in the analog domain. Consequently, the quality of the downconversion is not compromised by analog imperfections such as mismatch between the I and Q paths or the need to implement precise analog quadrature mixers. In fact, if the A/D converter's sampling frequency, f_S, is chosen to be 4 times the carrier frequency of the desired signal, f_{IF2}, then I/Q demodulation in the digital domain becomes a trivial matter of multiplication by 1, 0 and –1, as illustrated in Figure 2.8. A second advantage of digitizing at an intermediate frequency is that the problems of low frequency ($1/f$) noise and dc offset are avoided. However, as A/D conversion is moved away from baseband, the converter must sample at a higher rate, which entails a commensurate increase in power dissipation. Furthermore, since channel filtering is performed in the digital domain, the signal that must be digitized has a large dynamic range.

This dissertation explores the possibility of digitizing an IF signal with an oversampled bandpass sigma-delta ($\Sigma\Delta$) modulator. Oversampled bandpass converters can robustly

digitize the types of narrowband IF signals that arise in radios and cellular systems [50], [55], [56], [66]-[71]. Moreover, a receiver back-end that employs oversampled bandpass ΣΔ modulation is easily integrated because such converters can achieve the large dynamic range necessary for wireless systems without requiring trimming, or other steps incompatible with a standard, low-cost, CMOS process. However, in many such converters, the sampling frequency of the modulator is often restricted to be exactly four times the passband frequency. The architectural issues underlying this design choice are discussed in detail in the following chapters, but it can be noted immediately that the dynamic range of an $f_S/4$ bandpass A/D converter becomes increasingly constrained by circuit nonidealities at the high sampling rates needed to digitize signals at IF locations above 10 MHz. Consequently, for applications requiring a dynamic range of 70 dB or greater, the signal passband in previously reported $f_S/4$ modulators, has been located at a relatively low IF (under 5 MHz) [55], [69]. The emphasis in this research is to explore the performance limits of bandpass ΣΔ modulators at high sampling speeds such that narrowband (< 200 kHz) IF signals centered as high as 20 MHz can be digitized with over 70 dB of dynamic range.

2.4 Summary

This chapter has examined selectivity and integration issues in the back-end of a conventional superheterodyne radio receiver. Traditional fixed-frequency, highly-selective IF channel-select filters are seen to be a bottleneck inhibiting the full integration of the back-end of such a receiver. It is proposed that digitizing the signal at an intermediate frequency and implementing channel filtering in the digital domain is an effective means to circumvent this limitation. Previously reported lowpass A/D converters based on ΣΔ modulation have demonstrated the dynamic range needed to digitize baseband signals prior to channel filtering. However, in this approach, the quality of the baseband signal is susceptible to imperfections in the analog I/Q demodulation process. IF digitization by means of bandpass sigma-delta modulation is proposed as an alternative method that allows for the received signal to be digitized with a large dynamic range. Furthermore, in certain cases,

the subsequent digital I/Q demodulation can be implemented in a trivial manner that only requires multiplication by 1, 0 and –1. The next chapter reviews the principles of bandpass $\Sigma\Delta$ modulation.

Chapter

3

Bandpass ΣΔ Modulation

Digitization of the intermediate-frequency (IF) signal in a radio receiver can typically be accomplished with either a wideband Nyquist-rate analog-to-digital (A/D) converter or a converter that utilizes oversampling techniques and a noiseshaping architecture. Because the digitization of the IF signal is performed prior to channel-select filtering, the A/D converter must have a wide dynamic range in order to handle potential interferers, which may be 30-60 dB higher than the desired signal. Consequently, depending on the specifications of the particular wireless standard and the receiver architecture, the A/D converter may be required to have a dynamic range of 70 dB or greater.

It is problematic to design high-precision data converters with a traditional Nyquist-rate architecture in a modern submicron VLSI technology. Although submicron VLSI processes confer the benefits of smaller devices, increased transistor density, multiple layers of metal, and gate speeds on the order of tens of picoseconds, analog designs are encumbered because the process is optimized for digital circuits rather than precision mixed-signal analog applications. Due to short-channel effects and limitations imposed by velocity saturation, the intrinsic gain of the devices, $g_m r_o$, may be poor and the devices may be inherently noisier than their long-channel counterparts [99]. Often, these characteristics are poorly reflected in the models of the devices, which may then be inadequate for analog design. The designer may also be constrained by reduced supply voltages that preclude the use of certain analog circuit topologies such as cascoded amplifiers.

It is possible to utilize oversampling and noiseshaping principles to overcome the inherent limitations of the devices in a VLSI process. Noiseshaping techniques for wave-

form coding, with early applications to voiceband telecom, video encoders, and satellite telemetry, have been in existence since the early 1960s [9]-[11]. Through oversampling, feedback, and digital filtering, resolution in time is exchanged for that in amplitude. Therefore, it is possible to achieve a high dynamic range in spite of the poor device matching typical in VLSI processes. However, it was not feasible to implement a fully-integrated A/D converter in this manner until the late 1970s and early 1980s, when the density of CMOS technologies had improved to the point where the digital processing required became economical. The performance of noiseshaping converters has continued to increase with the scaling of VLSI technology, allowing them to progress through the increasingly demanding specifications of voiceband telecom, digital audio, ISDN, and channel digitization in wireless receivers [12]-[15].

In the past several years, the concept of lowpass noiseshaping has been extended to the bandpass regime whereby a narrowband signal centered around an intermediate frequency is directly digitized without first mixing the signal down to baseband [16], [17]. Through the design of an appropriate noise transfer function, the signal passband can be positioned at any location within the sampling bandwidth, $-f_s/2$ to $f_s/2$. In fact, certain classes of $f_s/4$ modulators are easily derived from existing lowpass topologies by applying a simple mathematical transformation to be described in Section 3.3.2. The simplicity of this approach is a strong motivation for adopting an architecture based upon a dc-to-$f_s/4$ transformation. However, system-level optimization with respect to factors such as spectral coloration and overload performance may demand more degrees of freedom than allowed by the transformation process. In addition, an unreasonably high sampling rate may be imposed on the analog circuitry if the modulator is to digitize a signal passband that is centered in the tens of MHz. These architectural issues are explored in depth in this chapter.

Before proceeding to a detailed discussion of bandpass sigma-delta (ΣΔ) modulation, a fundamental review of analog-to-digital conversion is presented, which is followed by an overview of oversampling and noiseshaping A/D techniques. Then, the remainder of the chapter is devoted to a broad study of bandpass noiseshaping architectures and a survey of

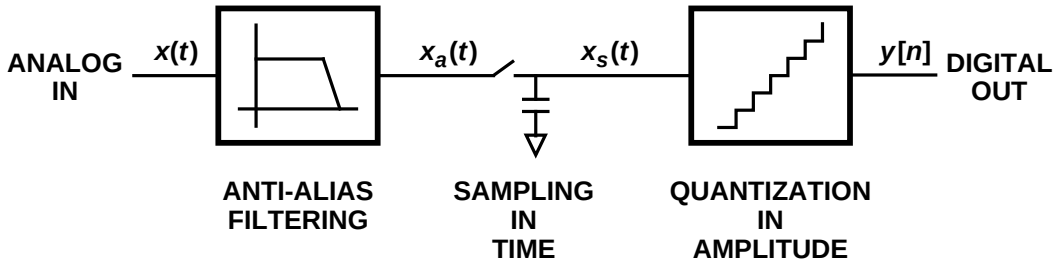


Figure 3.1: Fundamental operations comprising analog-to-digital conversion.

design methodologies. Transformations that operate on a lowpass prototype are discussed, and a generalized design technique that directly synthesizes the desired noiseshaping function is presented.

3.1 Nyquist-rate A/D Converters

Analog-to-digital conversion is the process of encoding an analog signal that is continuous in time and amplitude into a signal that is discrete with respect to time and quantized in amplitude. The fundamental operations comprising A/D conversion are illustrated in Figure 3.1. The analog input signal, $x(t)$, first passes through a bandlimiting lowpass filter, removing the signal components that lie above one-half of the sampling rate of the subsequent sampler. Otherwise, from the Nyquist sampling theorem [18], high frequency components of $x(t)$ would alias into the passband upon sampling, causing distortion that cannot be filtered or even distinguished from the original signal. Following the antialiasing filter, the bandlimited signal, $x_a(t)$, is sampled, thus yielding the discrete-time signal, $x_s(t) = x_a(nT_s)$, which is still continuous in amplitude. The sampled-data analog signal is then quantized in magnitude by the ensuing quantizer before being encoded into the output data signal, $y[n]$.

In some implementations of A/D converters, the sampling operation can be merged with the quantization process. For example, in an n-bit flash A/D converter, the analog

input signal is simultaneously compared to 2^n–1 reference voltages in a fully-parallel operation. Thus, in principle, flash A/D converters do not need to sample the signal prior to quantization because the sampling process can be performed implicitly by strobing a comparator bank.

3.1.1 Sampling

From the Nyquist sampling theorem, if there is to be no loss of information or aliasing distortion upon sampling, *x(t)* must be sampled at a frequency higher than twice the baseband cutoff frequency, f_b, which is defined as the cutoff frequency for the antialiasing filter as shown in Figure 3.2. In the frequency domain, the spectrum of the sampled signal, $x_s(t)$, is

$$X_s(f) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X_a(f - k f_s) \quad . \tag{3.1}$$

If the sampling frequency, f_s, is chosen to be at, or slightly higher than, the Nyquist rate, $2f_b$, then the converter is said to be a *Nyquist-rate converter*. However, the sampling rate can deliberately be chosen to greatly exceed the Nyquist rate in order to exploit the benefits of oversampling, to be described later in this chapter. In this case, the converter is referred to as an *oversampling converter*. When the passband extends from dc to f_b, the oversampling ratio, M, is defined as $M = f_s/(2 \times f_b)$, with $M = 1$ for a Nyquist-rate converter. The two classes of sampling are depicted in Figure 3.2.

3.1.2 Quantization

In principle, the sampling process does not result in any loss of information, provided that the sampling rate exceeds the Nyquist rate. However, this is not true of the quantization of the sampled signal because, in this non-reversible operation, a continuous range of amplitudes is mapped into a finite set of digital output codes. The transfer characteristic of a uniform quantizer with a gain of unity is illustrated in Figure 3.3(a), and the resulting saw-

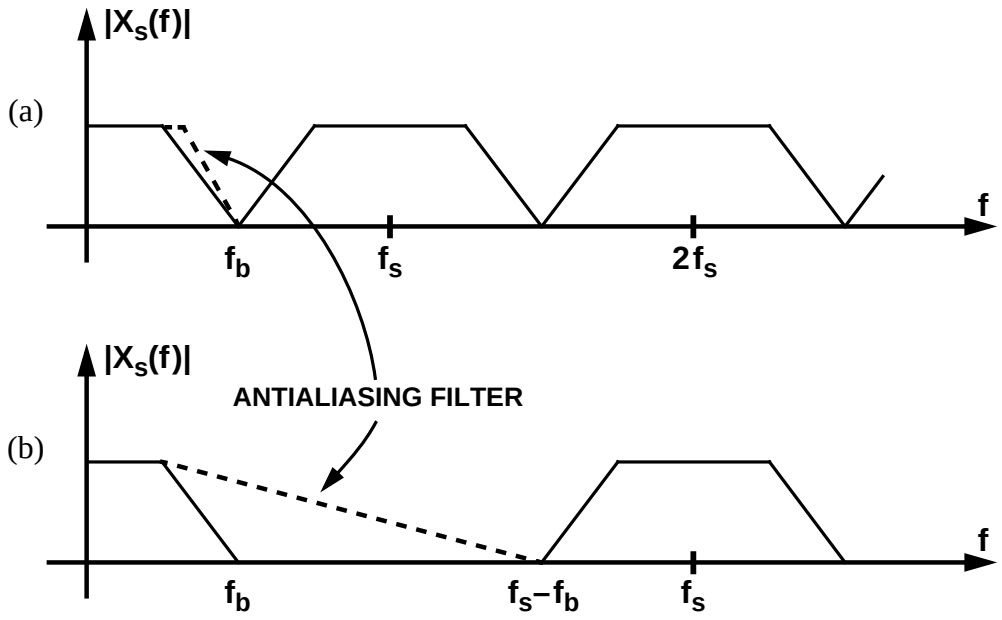


Figure 3.2: An analog signal that has been (a) sampled at the Nyquist rate, and (b) oversampled.

tooth quantization error is illustrated below in Figure 3.3(b). A unity-gain, uniform N-bit quantizer has 2^N quantization levels, and the step size, Δ, between quantization levels is

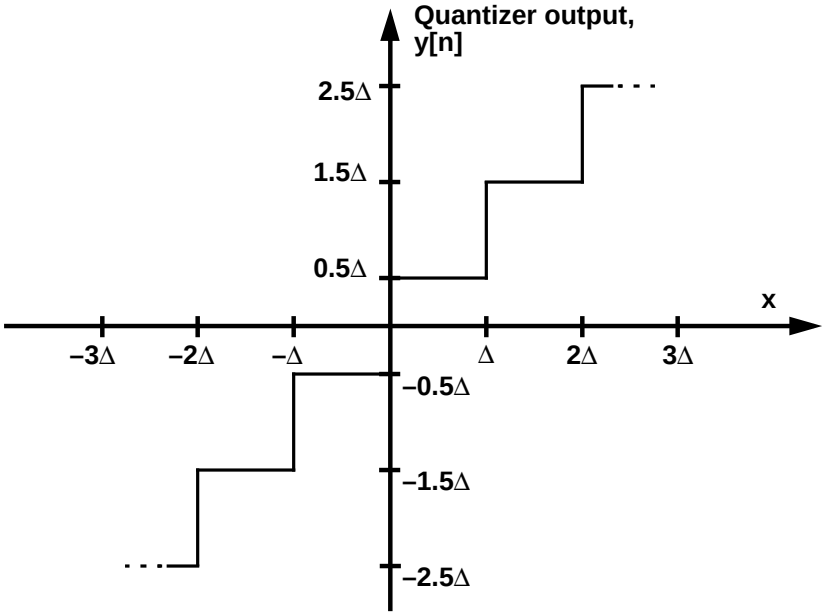
$$\Delta \equiv \frac{V_{REF}}{2^N - 1} \quad . \tag{3.2}$$

where V_{REF} is the full-scale input and output range of the quantizer.

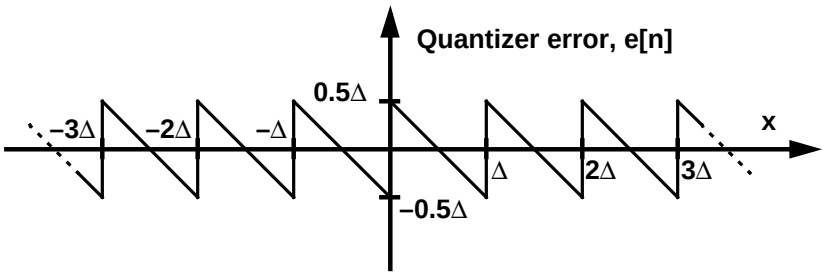
The output of the quantizer can be written as a sum of the input signal, $x[n]$, with the quantization error, $e[n]$, which is the result of a nonlinear operation, $q\{\cdot\}$, on $x[n]$:

$$y[n] \;=\; x[n] + e[n] \;=\; x[n] + q\{x[n]\} \quad . \tag{3.3}$$

However, it is difficult to analyze the effect of the quantizer using (3.3) because of the nonlinear and signal-dependent nature of the quantization error. To simplify the analysis, the quantization error, $e[n] = q\{x[n]\}$, is often approximated as additive white noise, and the



(a)



(b)

Figure 3.3: (a) Transfer characteristic and (b) error characteristic of a uniform quantizer.

quantizer is analyzed using statistical methods. Despite the deterministic nature of the quantizer error, it can be shown that the white noise approximation is valid if the following conditions are satisfied [19], [20]:

(1) the input signal never exceeds the input range of the quantizer,

(2) the quantizer has a large number of quantization levels,

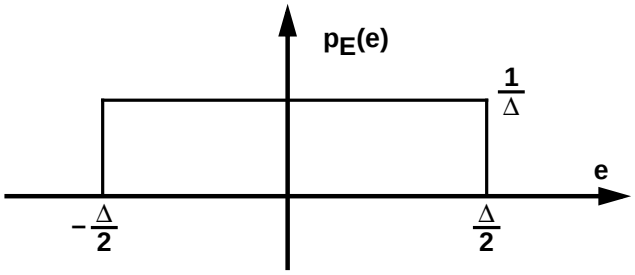


Figure 3.4: Probability density function of additive, white quantization noise.

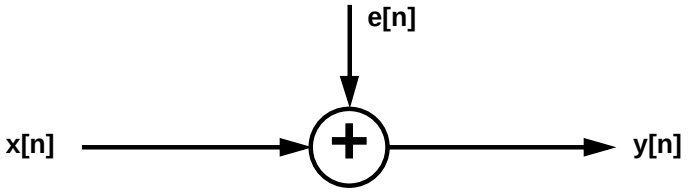


Figure 3.5: Linearized, stochastic model of quantizer.

(3) the input signal is active over many quantization levels, and

(4) the joint probability density of any two quantizer input samples is smooth.

Under these conditions, it is permissible to assume that the quantization error, $e[n]$, is distributed uniformly across its entire range, $-\Delta/2$ to $\Delta/2$, with the rectangular probability density function shown in Figure 3.4. The quantizer can then be replaced with the linearized stochastic model of Figure 3.5. The variance of the quantizer error, $e[n]$, is

$$\sigma_e^2 = \int_{-\infty}^{\infty} e^2 p_E(e)de = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12} . \tag{3.4}$$

The signal-to-quantization noise ratio is defined as the ratio of the input signal power, σ_x^2, to the variance of the quantization error, σ_e^2. Given that the N-bit quantizer has 2^N

quantization levels, a full-scale sinusoidal input to the quantizer has an amplitude of $2^{N-1}\Delta$ and a corresponding signal power of $2^{2N-3}\Delta^2$. Therefore, if the noise floor of the A/D converter is determined primarily by quantization noise, then the A/D converter will have a useful input signal range encompassing full-scale input signal levels down to an input signal level that yields a signal-to-quantization noise ratio of one. This is defined as the dynamic range of the A/D converter,

$$DR = \frac{\sigma_x^2}{\sigma_e^2} = \frac{2^{2N-3}\Delta^2}{\frac{\Delta^2}{12}} = \frac{3}{2} \times 2^{2N} . \tag{3.5}$$

The familiar expression relating the dynamic range to the number of bits of a uniform *N*-bit quantizer is found by taking the *log* of (3.5), which leads to

$$10 \log DR = 6.02 \times N + 1.76 dB \tag{3.6}$$

Therefore, if the resolution of an A/D converter is limited by quantization noise, then its dynamic range increases by approximately 6 dB with every additional bit of resolution. In practical implementations, the minimum resolvable signals may be limited by circuit noise or thermal noise rather than quantization noise. Nevertheless, in such cases, the dynamic range is defined similarly, with the lower limit established by an input signal level that yields a signal-to-noise ratio of one.

3.1.3 Limitations of the Additive White Noise Model

In many cases in this research, the nature of the input signal and the quantizer violate one or more of the assumptions needed to justify the modeling of the quantizer as a source of additive white noise. Because the quantization noise is in fact correlated with the input signal, the spectrum of the quantizer output can contain discrete tones that are not predicted by the white noise model [21]. This correlation is particularly strong in the case of the two-level, or 1-bit, quantizers used in the feedback modulators to be described later in this chapter. However, it is nevertheless useful to model the quantizer in this manner to

predict the performance of an A/D converter, despite the failure of the system to adhere to the stipulations of the model. In particular, even though the 1-bit quantizer violates the conditions of the model, the white noise quantizer model still allows for an accurate estimate of the dynamic range of a modulator that is comprised essentially of a 1-bit quantizer embedded in a feedback loop. In such cases, the only justification for modeling the quantizer as an additive white noise source is that behavioral simulations of the system confirm the estimate of the dynamic range arrived at with the use of this model.

3.1.4 Limitations of Nyquist-Rate A/D Converters

There are many architectures for Nyquist-rate A/D converters, each of which embodies various tradeoffs among bandwidth, power dissipation, area, and dynamic range requirements. A thorough review of many architectures is presented in [22], [23]. A common limiting factor in all Nyquist-rate architectures is that some operation such as comparison, amplification, or subtraction must be performed to the overall precision of the converter. This typically translates into the need for precise component matching unless special calibration, error-correction, or trimming techniques are used, with attendant penalties in die area, power dissipation, or manufacturing cost. With careful layout techniques, matching of 0.3% can be routinely achieved in modern CMOS processes, and matching as good as 0.1% has been observed [30]. However, it is important to note that even with 0.1% matching, the resolution of an uncalibrated and untrimmed Nyquist-rate converter is limited to only 10 bits.

A steep antialiasing filter must also precede any Nyquist-rate A/D converter. This bandlimiting filter rejects frequency components of the signal located above one-half of the sampling frequency in order to prevent aliasing distortion. However, to allow for a large signal bandwidth, the filter's stopband corner frequency must also be near one-half of the sampling frequency. Thus, as depicted in Figure 3.2(a), the antialiasing filter must have a sharp transition band, which typically introduces phase distortion in signal components located near the cutoff frequency. Furthermore, it is difficult to implement precise analog filters with multiple poles in a VLSI technology due to a lack of high-Q inductors

and well-defined, stable resistor and capacitor values. Circuit noise and distortion in active implementations of continuous-time filters, such as g_m/C topologies, often limit their utility to applications that only require a low- to medium dynamic range [24]-[29]. This becomes increasingly true at the low supply voltages, 2.5 V to 3.3 V, typical of submicron technologies, in which the large signal swings necessary for a high dynamic range directly conflict with the linearity requirements of the filter. Finally, the precisely defined poles and zeros of any high-order continuous time filter will be subjected to a wide range of environmental and processing fluctuations that can potentially disturb the passband response and degrade the sharp selectivity of the filter. Thus, a compensatory automatic tuning scheme may be necessary to constrain the variations of the filter's frequency response [29].

3.2 Oversampled A/D Converters

By exploiting the speed of a VLSI technology, it is often possible to sample the input signal at a rate much higher than the Nyquist rate. This oversampling offers the immediate advantage of relaxing the requirement for a steep transition band on the antialiasing filter, as illustrated in Figure 3.2(b). However, as discussed in the following section, oversampling by itself leads to only modest improvements in resolution of the converter. If the quantizer is also embedded in a feedback loop, it is possible to significantly increase the resolution of a converter beyond what can be achieved simply by oversampling.

It is important to note that the quantization process in an oversampled converter employing feedback differs fundamentally from that in a Nyquist-rate converter. It is not necessary to quantize the signal in an oversampled converter to the full resolution of the converter because each sample of the input signal does not correspond to only one output sample. Rather, in the digital filter that follows the oversampled converter, many coarsely quantized samples are processed to yield a more precise estimate of the analog input signal at a lower sampling rate. Thus, each output sample depends on a long sequence of input samples. In many cases, single-bit quantization is sufficient in an oversampled feedback modulator.

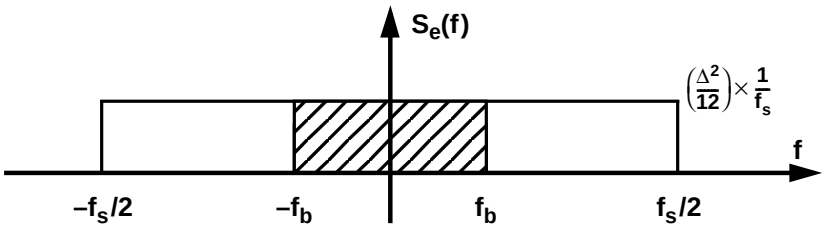


Figure 3.6: Power spectral density of quantization noise when the input signal is oversampled.

3.2.1 Oversampling

The resolution of a Nyquist-rate converter can be increased in a straightforward manner by operating the converter at a sampling rate in excess of the Nyquist rate. As found in Section 3.1.2, if the quantization error is modeled as an additive white noise source, the total noise power, $\Delta^2/12$, is uniformly distributed across the sampling bandwidth, $-f_s/2$ to $f_s/2$. When the input is oversampled, the signal bandwidth, $-f_b$ to f_b, is only a fraction of the sampling bandwidth, as depicted in Figure 3.6. Therefore, in the presence of oversampling, the inband power of the quantization noise can be expressed as

$$\sigma_e^2 = \frac{\Delta^2}{12} \times \frac{1}{M} \tag{3.7}$$

where M is the oversampling ratio. Thus, the quantization noise power, σ_e^2, is reduced by a factor of M, and the maximum achievable dynamic range increases by 3 dB, or 1/2 bit, per octave of oversampling.

Simply increasing the sampling rate does not significantly improve the dynamic range of a coarsely quantized Nyquist-rate converter. For example, in order to improve the resolution of a Nyquist-rate converter with a 22 kHz audio signal bandwidth from 8 bits to 16 bits, it is necessary to increase the sampling frequency of the converter from 44 kHz to over 2.8 GHz. Also, the disturbing possibility exists that due to the correlation of the quantization error with the input signal, it is possible to place the converter in a state where no degree of oversampling will improve its resolution. One example of such a situation is

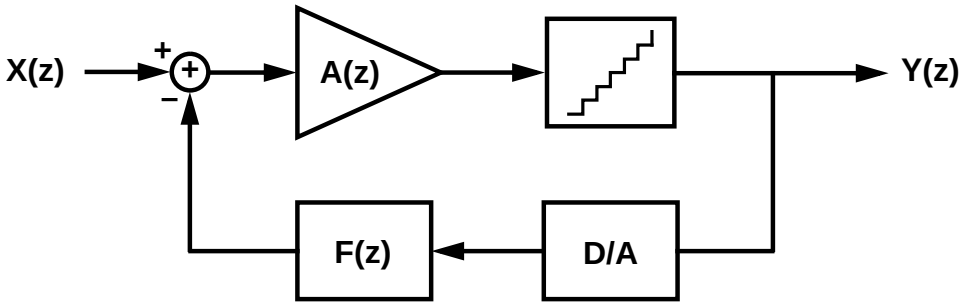


Figure 3.7: Feedback modulator.

when a dc input is applied to the converter. Fortunately, as reviewed in the following sections, the inband quantization noise power can be suppressed dramatically by embedding the quantizer in a feedback loop. In this manner, the quantization noise is spectrally shaped such that the bulk of it is moved out of the signal passband. The structure formed by enclosing a quantizer in a feedback loop with filters in either, or both, the forward and return paths is commonly referred to as a feedback modulator.

3.2.2 Feedback Modulators

The general structure of a feedback modulator is illustrated in Figure 3.7, which shows a quantizer embedded in a loop with a digital-to-analog (D/A) converter in the feedback path. The transfer function of the filter in the forward path of the modulator is denoted $A(z)$, while the filter in the feedback path has the transfer function $F(z)$. The output of a feedback modulator is described in the z-domain by

$$Y(z) = \frac{A(z)}{1 + A(z)F(z)} \cdot X(z) + \frac{1}{1 + A(z)F(z)} \cdot E(z) \,. \tag{3.8}$$

Feedback modulators are commonly described in terms of two broad classes based on the characteristics of the forward-path and feedback-path transfer functions. In *predictive* modulators, the feedback filter, $F(z)$, has a large gain in the signal passband and provides an estimate of the input signal, which is then subtracted from the actual input to the modu-

lator, $X(z)$. If the predicted value is close to the input value, the quantizer input will be small, allowing the use of a quantizer with a small input range. In effect, by encoding the rate of change of a signal rather than the signal itself, a *predictive* modulator can employ a quantizer with a small step size and a commensurately small quantization error. In contrast, *noiseshaping* modulators do not reduce the magnitude of the quantization noise. Instead, a large frequency-dependent gain in the forward path, $A(z)$, is used to spectrally shape the quantization noise and suppress it in the signal passband. Most of the power in the quantization noise is moved into the stopband where it is removed by a digital filter that follows the modulator.

In a predictive modulator, both the input signal and the quantization noise undergo spectral shaping [31]-[34]. This fact has important implications in the practical implementation of feedback modulators. From (3.8) it is seen that the signal transfer function, $STF(z)$, of a feedback modulator is

$$STF(z) = \frac{A(z)}{1 + A(z)F(z)} \quad . \tag{3.9}$$

Since the passband gain of the feedback filter, $F(z)$, is very high in a predictive modulator, the signal transfer function is approximately $1/F(z)$. Therefore, the digital filter that follows a predictive modulator must apply an inverse transfer function, $\hat{F}(z)$, which is a digital approximation of the analog feedback filter transfer function $F(z)$, to the output of the modulator in order to recover the input signal. Mismatch between $\hat{F}(z)$ and $F(z)$ presents an immediate limitation because the nonidealities in the analog circuits that are the root cause of the mismatch cannot be predicted *a priori*. Furthermore, mismatch-related errors are greatly amplified because the passband gain of $F(z)$ and $\hat{F}(z)$ is very high.

In noiseshaping modulators, only the quantization noise is spectrally shaped [13], [14], [35]-[37]. The forward filter, $A(z)$, has a large passband gain and the feedback filter, $F(z)$, is independent of frequency in the passband. Therefore, the signal transfer function, (3.9), reduces to a constant in the passband, and the digital filter that follows a noiseshaping modulator must only reject the large, out-of-band quantization noise without altering the

frequency response in the signal passband. The performance of a noiseshaping modulator is not limited by the need to match a digital decoding filter $\hat{F}(z)$, to the analog feedback filter, $F(z)$, in the modulator. For this reason, *noiseshaping* topologies are preferred if the feedback modulator is to be implemented with analog circuitry. This research work focuses exclusively on noiseshaping topologies.

At this point, it is important to note that in the development of noiseshaping techniques it was usually presumed that the signal passband was situated at baseband. However, spectral shaping of noise is not restricted to the lowpass domain. Rather, through an appropriate choice of the forward and feedback transfer functions, $A(z)$ and $F(z)$, it is possible to shape the bulk of the quantization noise power away from any region in the sampling bandwidth, $-f_s/2$ to $f_s/2$. The concept of bandpass noiseshaping will be developed later in this chapter following the initial discussion of lowpass noiseshaping.

3.2.3 Lowpass Sigma-Delta (ΣΔ) Modulation

In noiseshaping topologies, the forward path filter is designed to have a large gain in the passband in which the quantization noise is to be suppressed. From Figure 3.7, it follows that if $F(z)$ is chosen to be 1, the z-domain expression for the output can written as

$$Y(z) = \frac{A(z)}{1 + A(z)} \cdot X(z) + \frac{1}{1 + A(z)} \cdot E(z) \tag{3.10}$$

where $X(z)$ and $E(z)$ are the z-transforms of the input signal and quantization error, respectively. Therefore, if the quantization noise is to be suppressed in the baseband, $A(z)$ must have a large dc gain. There are many transfer functions that satisfy this condition and could be used to implement a noiseshaping modulator, but one class of transfer functions comprised of integrators is especially suited for VLSI implementation because the analog circuits required to implement the transfer function are simple and robust.

A z-domain representation of a first-order ΣΔ modulator is depicted in Figure 3.8. The modulator is comprised of a subtraction node, a discrete-time integrator, and a 1-bit quantizer. The quantization noise is represented by the additive term, $E(z)$. The integrator

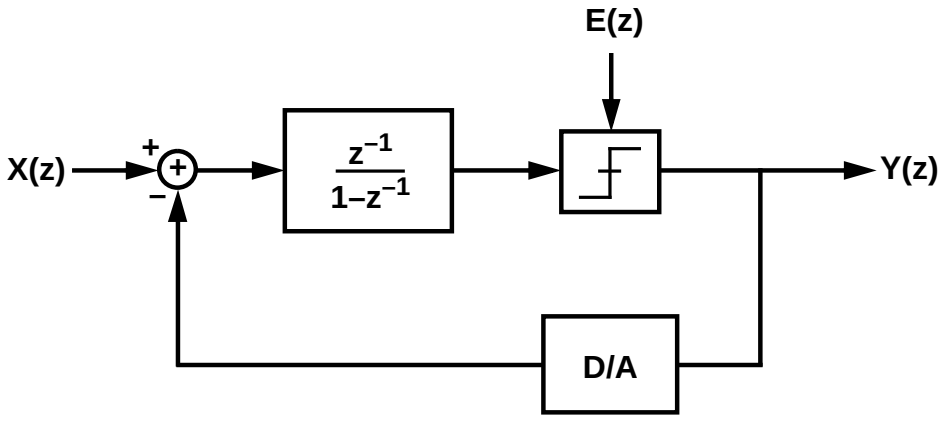


Figure 3.8: First-order lowpass ΣΔ modulator.

ideally provides an infinite gain at dc, which, from (3.10), is necessary to suppress the quantization noise at baseband. In a similar fashion, a simple *bandpass* sigma-delta modulator can be derived from the first-order lowpass prototype by replacing the integrator with a resonator that provides an infinite gain in the passband of interest.

A multibit quantizer can be embedded in the feedback loop in order to improve the dynamic range of the modulator for a given oversampling ratio, or to reduce the oversampling ratio for a given dynamic range [38]-[41]. However, the multilevel D/A converter in the feedback path is then required to have a linearity equal to or exceeding the overall linearity of the modulator. Otherwise, nonlinearity in the feedback D/A converter will introduce harmonic distortion directly at the input to the modulator. Dynamic element matching techniques can be used to randomize and decorrelate the error from the nonideal D/A converter, thus causing the error to appear as an additive white noise, rather than as harmonic distortion, at the expense of increased power and complexity in the modulator [42]-[44]. Therefore, ΣΔ modulators are often implemented using inherently linear 1-bit quantizers and 1-bit D/A converters and are operated at oversampling ratios high enough to guarantee the suppression of the large quantization noise associated with a 1-bit quantizer. Single-bit D/A converters can still contribute gain and offset errors in the feedback path, but ΣΔ modulators are relatively insensitive to these perturbations [14].

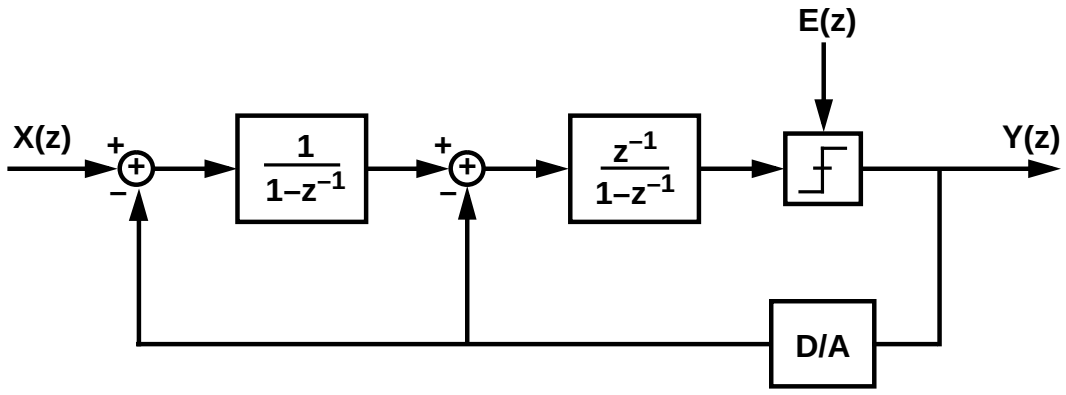


Figure 3.9: Second order lowpass ΣΔ modulator.

In the *z*-domain representation of the first-order ΣΔ modulator, Figure 3.8, the quantization noise is represented by an additive white noise source, $E(z)$. As explained in Section 3.1.3, the 1-bit quantizer topology strongly violates the assumptions of the additive white noise model. In particular, the quantization noise is highly correlated with the input signal. However, it is nevertheless useful to begin the analysis using this model to estimate the dynamic range of the modulator. The results are then confirmed through computer simulations of a behavioral model of the modulator, hereafter referred to as *behavioral simulations*. The 1-bit D/A converter is assumed to be ideal and does not introduce any additional noise. In the *z*-domain, the output of the first-order lowpass modulator is

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \ , \tag{3.11}$$

which consists of the input, *X(z)*, delayed by one sample period, plus a first-order highpass shaping of the additive quantizer noise, *E(z)*.

If the quantizer in a first-order lowpass ΣΔ modulator is itself replaced by a first-order ΣΔ modulator, and the first-stage integrator is implemented without a delay, then the second-order, lowpass modulator of Figure 3.9 results. The output of the second-order, lowpass, noise-differencing lowpass modulator is

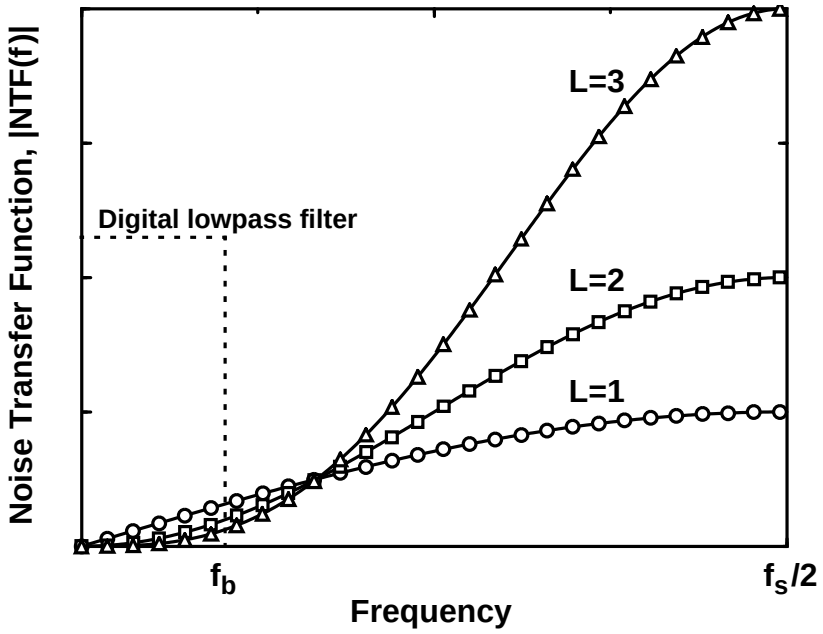


Figure 3.10: First-, second-, and third-order lowpass noise transfer functions.

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 E(z) \ . \tag{3.12}$$

The second-order shaping of *E(z)* suppresses the quantization noise more effectively in the baseband than first-order shaping. In general, as the order of the noise shaping increases, the level of quantization noise present in the signal passband decreases and the out-of-band noise increases more than commensurately. The trend of noiseshaping behavior as the order of the modulator increases is qualitatively depicted in Figure 3.10. Although the quantization noise is suppressed more effectively through the use of higher-order modulators, the order of a modulator cannot be increased arbitrarily because it is difficult to guarantee the stability of third- and higher-order single-bit modulators [45], [46]. For certain combinations of input signals and initial conditions, the internal states of the higher-order modulator can continue to grow without bound, eventually saturating the analog circuitry. If this condition persists after the input signal to the modulator is removed, additional circuitry is needed to sense and reset the internal modulator states

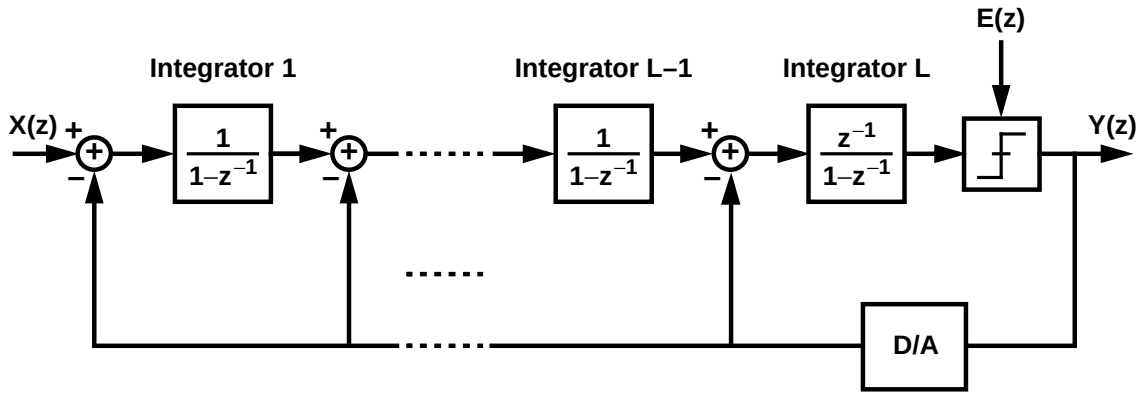


Figure 3.11: L^{th}-order lowpass ΣΔ modulator.

[48]. Special design procedures can be followed in order to guarantee that the modulator can recover when overdriven at the input or when initially placed in an overload state. Alternatively, higher-order modulators can be implemented by cascading first- and second-order modulators, which are known to be stable [39], [49].

If the noise-differencing lowpass ΣΔ modulator topology is extended to the L^{th}-order case, as illustrated in Figure 3.11, the noise transfer function is

$$NTF(z) = (1 - z^{-1})^L \quad , \tag{3.13}$$

which in the frequency domain is

$$NTF(f) = NTF(z)\Big|_{z = e^{j2\pi f T_s}} = (1 - e^{-j2\pi f T_s})^L \quad . \tag{3.14}$$

Under the additive white noise model, the power of the quantization noise, $E(z)$, is found from (3.4) to be $\Delta^2/12$, and is distributed uniformly in the sampling bandwidth, $-f_s/2$ to $f_s/2$. Therefore, the power spectral density of the quantization noise is

$$S_e(f) = \frac{P_e}{f_s} = \frac{\Delta^2}{12} \times \frac{1}{f_s} \quad , \qquad -\frac{f_s}{2} < f < \frac{f_s}{2} \quad , \tag{3.15}$$

and the spectral density of the shaped quantization noise is

$$S_Q(f) = |NTF(f)|^2 \cdot S_E(f) = (2\sin(\pi f T_s))^{2L} \cdot \frac{\Delta^2}{12} \times \frac{1}{f_s} \ . \tag{3.16}$$

By integrating $S_Q(f)$ over the band of interest, the power of the quantization noise present in the signal band can be found. The out-of-band quantization noise is assumed to be rejected by a lowpass digital filter that follows the modulator. Since $f_b << f_s$, the integral can be evaluated under the approximation $\sin(x) \approx x$ to yield an inband quantization noise power equal to

$$P_Q = \int_{-f_b}^{f_b} S_Q(f)df \approx \left(\frac{\pi^{2L}}{2L+1}\right) \times \left(\frac{1}{M^{2L+1}}\right) \times \frac{\Delta^2}{12} \ , \qquad M >> 1 \ . \tag{3.17}$$

For this 1-bit modulator, a full-scale sinusoid has a peak-to-peak amplitude equal to the quantization step size, Δ, and a power equal to $\Delta^2/8$. Hence, the dynamic range of an L^{th}-order, noise-differencing lowpass $\Sigma\Delta$ modulator with an oversampling ratio of M is

$$DR = \frac{3}{2} \cdot M^{2L+1} \cdot \frac{2L+1}{\pi^{2L}} \tag{3.18}$$

where, as defined previously, M is equal to the ratio of the sampling frequency to the Nyquist frequency, $M = f_s/(2 \times f_b)$.

3.3 Bandpass Noiseshaping

The principles of noiseshaping can be extended from the lowpass case, in which the quantization noise is suppressed around dc, to the more general bandpass case where the quantization noise is attenuated in a narrow passband centered at an intermediate frequency. As alluded to in Section 3.2.3, the quantization noise in a noiseshaping modulator can be suppressed in any narrowband portion of the sampling bandwidth by designing the transfer function of the forward path filter, $A(z)$ in Figure 3.7, to have a resonant peak in

the signal passband. The feedback filter, $F(z)$, is assumed to have a passband gain of 1. Because the gain of $A(z)$ is ideally infinite at its peak, it is seen from (3.8) that the denominator of the noise transfer function,

$$NTF(z) = \frac{1}{1 + A(z)F(z)} , \tag{3.19}$$

is large in a narrow region around the resonant peak. Therefore, the magnitude of the noise transfer function, (3.19), is quite small in the signal passband.

The requirement for a high quality forward path filter in a bandpass noiseshaping modulator suggests an interesting tradeoff when considered from the system-level perspective of radio receiver design. Recall from Chapter 2 that one strong motivation for performing a bandpass A/D conversion in a receiver is to eliminate the need for highly selective IF filters in its back-end circuitry. However, in a bandpass sigma-delta modulator, it appears that the requirements on IF filtering have simply been moved inside the modulator feedback loop, since the forward path filter, $A(z)$, must have a sharp and well-defined resonance at the IF center frequency. Fortunately, $A(z)$ can typically be synthesized by cascading two or more second-order biquadratic filters, which can have loosely defined frequency responses away from their resonant center frequency. Furthermore, a resonator can be implemented such that its center frequency remains invariant with respect to its sampling frequency despite coefficient errors arising from circuit nonidealities or mismatches. In contrast, for reasons discussed in Section 2.1.2 and Section 3.1.4, it is much more difficult to implement a multiple-pole IF filter that has a well-controlled and stable response in a narrow passband region, together with a steep transition band and a large attenuation in the stopband.

It is implicit in this discussion of bandpass noiseshaping that the modulator is digitizing a real-valued signal that is symmetric about dc. Likewise, the signal and noise transfer functions of the modulator are assumed to include conjugate pairs of poles and zeros, which insures that the frequency response of the modulator extends symmetrically across dc from $-f_s/2$ to $f_s/2$. However, the principles of bandpass noiseshaping can be generalized

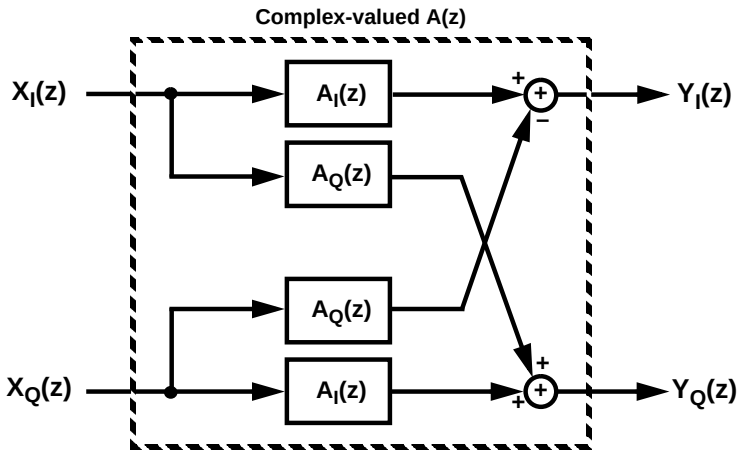


Figure 3.12: Synthesizing a complex-valued transfer function from real-valued building blocks.

to enable the digitization of complex signals by synthesizing complex-valued transfer functions in the forward and feedback path of the modulator. A complex filter can be realized using real-valued filter blocks as illustrated in Figure 3.12. A bandpass modulator comprised of complex filters can then digitize a complex-valued input signal, $x_I[n] + jx_Q[n]$, generating two output data streams from quantizers in both the inphase (I) and quadrature (Q) branches [50], [51].

The design and analysis of bandpass ΣΔ modulators share much in common with their lowpass counterparts. In fact, many advantages inherent to the architecture of lowpass modulators are preserved when the noiseshaping function is transformed into the bandpass domain. For example, in both cases, the modulators benefit from the intrinsic linearity of the single-bit quantizer and D/A converter in the feedback loop. Also, both types of modulators exhibit relatively low sensitivity to variations in the system parameters and implementation nonidealities such as comparator hysteresis. These advantages translate to robust analog circuit implementations of the modulators. However, the design of bandpass modulators also entails specific hazards that are only shared to a lesser degree with lowpass modulators. In one particularly important example, the out-of-band spectrum in both

lowpass and bandpass modulators is contaminated by the presence of strong spectral tones. In lowpass modulators, high-level tones have been reported near $f_s/2$ [52], [53], which are easily rejected by the digital lowpass filter that follows the modulator. However, in bandpass modulators, strong tones have been reported near dc as well as $f_s/2$ [54]. Although these tones also lie in the stopband region, they can potentially degrade the noise and distortion characteristics of the bandpass modulator by mixing with the input signal and falling into the passband. This hazard can be partially defused by centering the signal passband away from $f_s/4$, but the architecture of the modulator then becomes considerably more complicated, and it may be difficult to guarantee the stability of the modulator. The remainder of this section is devoted to a discussion of these hazards and other design issues relevant to modulators that center the noise suppression region at an intermediate frequency between dc and $f_s/2$.

3.3.1 Passband Location

The passband of a bandpass modulator can be situated anywhere in the sampling bandwidth from $-f_s/2$ to $f_s/2$. However, there are several compelling advantages gained by forcing the passband to lie exactly at one-quarter of the sampling frequency. First, comparatively simple analog circuits can be used to implement the modulator, which may be a necessity if the modulator is to operate at high sampling frequencies. Second, one class of $f_s/4$ bandpass topologies can easily be derived from lowpass prototypes with a simple mathematical transformation to be described in Section 3.3.2. Finally, as discussed in Section 2.3, *I* and *Q* demodulation is especially straightforward when the passband is centered at $f_s/4$. The tradeoff for this architectural choice is that the dynamic range of the modulator becomes increasingly constrained by circuit nonidealities at the high sampling rates needed to digitize signals at IF locations above 10 MHz. A detailed discussion of the analog circuits comprising the modulator is delayed until Chapter 6.

The choice of passband may also be influenced by the requirements imposed on the antialiasing filter that precedes the modulator. Figure 3.13 illustrates how the transition band of the filter becomes sharper as the passband moves away from dc. In order to avoid

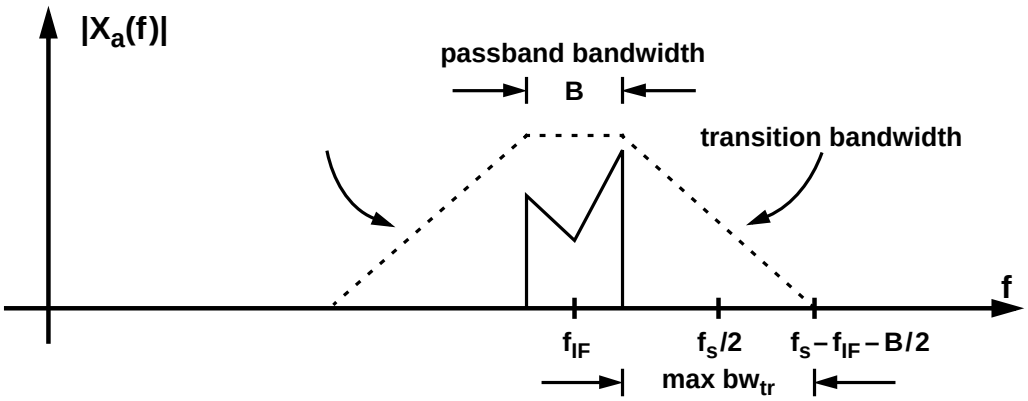


Figure 3.13: Antialiasing filtering in a bandpass modulator.

aliasing distortion upon sampling, the bandwidth of the transition region, bw_{tr}, is limited to

$$\begin{aligned} bw_{tr} &< f_s - f_{IF} - \frac{B}{2} - \left(f_{IF} + \frac{B}{2} \right) \\ &< f_s - 2 f_{IF} - B \end{aligned} \tag{3.20}$$

where B is the width of the passband and f_{IF} is the passband center frequency. For lowpass modulators, the passband is centered at dc, and the baseband bandwidth extends from dc to f_b. Thus, if $f_{IF} = 0$ and f_b is defined to equal $B/2$, then (3.20) reduces to the familiar lowpass constraint, which states that the transition band can only extend from the edge of the baseband, $B/2$, to a frequency equal to the sampling frequency minus the baseband edge frequency, $f_s - B/2$ [57].

If the ratio of the transition band to the passband is relatively high, as is the case when the passband is situated at, or below, $f_s/4$, then simple bandpass filters can perform the necessary antialiasing filtering. Such bandpass filters can be designed by applying the continuous-time, lowpass-to-bandpass transformation [58],

$$H_{bandpass}(s) = H_{lowpass}(\hat{s})\Big|_{\hat{s} = \frac{1}{\eta}\left(s + \frac{\omega_o^2}{s}\right)}, \tag{3.21}$$

to a lowpass prototype filter. In (3.21), ω_o is the center frequency of the bandpass filter, and η is a scaling factor that affects the width of the passband. The passband edges of the new bandpass filter are

$$\omega_{bp1},\omega_{bp2} = \pm\frac{\omega_{lp}\eta}{2} + \sqrt{\omega_o^2 + \left(\frac{\omega_{lp}\eta}{2}\right)^2} \tag{3.22}$$

where ω_{lp} is the edge of the passband in the prototype lowpass filter. As the passband center frequency approaches $f_s/2$, the allowable transition region bandwidth diminishes according to (3.20), with the cutoff requirements for the antialiasing filter eventually approaching those imposed on the bandlimiting filter that precedes Nyquist-rate converters.

3.3.2 Transformation from dc to $f_s/4$

One class of bandpass modulators that centers the passband at $f_s/4$ can be easily derived by applying the mathematical transformation

$$z^{-1} \rightarrow -z^{-2} \tag{3.23}$$

to the L^{th}-order, noise-differencing lowpass architecture depicted in Figure 3.11 [55], [56]. This dc-to-$f_s/4$ transformation effectively replaces the integrators in an L^{th}-order, lowpass prototype with two-pole, bandpass resonators that ideally realize an infinite gain at $f_s/4$. If (3.23) is applied to a delaying, discrete-time integrator, then the resulting bandpass resonator has the transfer function

$$H_{bp}(z) = \left.\frac{\hat{z}^{-1}}{1-\hat{z}^{-1}}\right|_{\hat{z}^{-1} = -z^{-2}} = \frac{-z^{-2}}{1+z^{-2}} \ . \tag{3.24}$$

In the same manner, if the second-order, lowpass modulator of Figure 3.9 is transformed to the bandpass domain via (3.23), the canonical, fourth-order, $f_s/4$ bandpass modulator depicted in Figure 3.14 results. This topology is referred to as being canonical because it is derived directly from the original, second-order topology described by Candy for low-

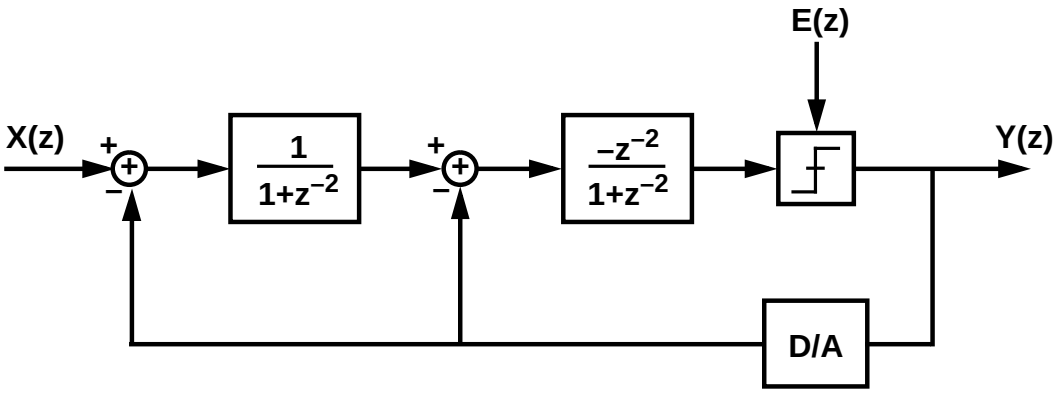


Figure 3.14: Canonical, fourth-order, $f_s/4$ ΣΔ modulator.

pass noiseshaping [13]. In the z-domain, the output of the canonical, fourth-order, $f_s/4$ modulator is

$$Y(z) = -z^{-2}X(z) + (1 + z^{-2})^2 E(z) \quad . \tag{3.25}$$

The dc-to-$f_s/4$ transformation, (3.23), has effectively doubled the number of zeros of the lowpass noise transfer function and rotated these zeros in the z-plane from $z = 1$ to $z = \pm j$, as depicted in Figure 3.15. In the frequency domain, the noise suppression region has been shifted from dc to $\pm f_s/4$.

In the case of bandpass modulators, there can be some confusion involved in specifying the order of the modulator, which refers to the number of poles in the noise transfer function, $NTF(z)$. With this definition, it is clear that the $f_s/4$ modulator of Figure 3.14 is a fourth-order modulator. But because there are only two zeros in the noise transfer function at $f_s/4$, with the other two zeros located at $-f_s/4$, the quantization noise is only suppressed with a second-order bandstop transfer function in the signal passband. For lowpass modulators, there is no discrepancy between the order of the noise transfer function and the number of zeros that suppress the quantization noise around dc; they are equivalent. But, for bandpass modulators, it should be understood that the order of the modulator strictly refers to the number of poles in $NTF(z)$.

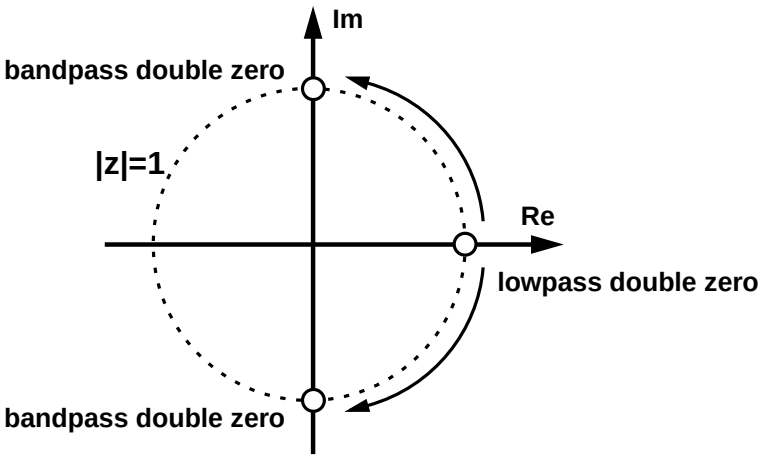


Figure 3.15: Zeros of the noise transfer function of a fourth-order, $f_s/4$ modulator.

In this work, canonical $f_s/4$ bandpass topologies that are derived using the dc-to-$f_s/4$ transformation of (3.23) are the topologies of choice because the resulting modulators are especially suited for high-speed applications. In particular, these modulators have the property that they can be readily implemented using a two-path architecture. By partitioning the bandpass modulator into two independent, time-interleaved highpass modulators, the demand for rapid settling in the analog circuits is relaxed by a factor of two. Furthermore, the constituent path filters can be implemented using relatively simple circuitry. These advantages are of importance to high-resolution modulators that operate at sampling frequencies in the tens of MHz, which is necessary if the modulator is to digitize signals located at traditional radio intermediate frequencies. The two-path design issues are discussed in depth in Chapter 5.

The dynamic range of a bandpass modulator can be estimated in the same manner used to calculate that of a lowpass modulator. If the $f_s/4$ architecture illustrated in Figure 3.14 is extended to the $2L^{th}$-order case by applying (3.23) to the L^{th}-order, noise-differencing lowpass architecture depicted in Figure 3.11, the resulting noise transfer function is

$$NTF(z) = (1 + z^{-2})^L \ , \tag{3.26}$$

which in the frequency domain, can be written as

$$NTF(f) = NTF(z)\Big|_{z = e^{j2\pi f T_s}} = (1 + e^{-j4\pi f T_s})^L \ . \tag{3.27}$$

Assuming that the quantization noise, $E(z)$, is additive, with a total power of $\Delta^2/12$ that is distributed uniformly in the sampling bandwidth, $-f_s/2$ to $f_s/2$, the power spectral density of $E(z)$ is

$$S_e(f) = \frac{\Delta^2}{12} \times \frac{1}{f_s} \ , \qquad -\frac{f_s}{2} < f < \frac{f_s}{2} \ . \tag{3.28}$$

The quantization noise is shaped by the transfer function

$$\left|NTF_e(f)\right|^2 = (2\cos 2\pi f T_s)^{2L} \ . \tag{3.29}$$

The power of the quantization noise in the passband can be found by integrating the power spectral density of the shaped quantization noise,

$$S_Q(f) = (2\cos 2\pi f T_s)^{2L} \cdot \frac{\Delta^2}{12} \times \frac{1}{f_s} \ , \qquad -\frac{f_s}{2} < f < \frac{f_s}{2} \ , \tag{3.30}$$

over the signal bandwidth centered at $f_s/4$. The out-of-band quantization noise is assumed to be rejected by a digital filter that follows the modulator. Since $B << f_s$, the integral can be evaluated under the approximation $\sin(x) \approx x$ to yield an inband quantization noise power equal to

$$P_Q = \int_{-\frac{f_s}{4}-\frac{B}{2}}^{-\frac{f_s}{4}+\frac{B}{2}} S_Q(f)df + \int_{\frac{f_s}{4}-\frac{B}{2}}^{\frac{f_s}{4}+\frac{B}{2}} S_Q(f)df$$

$$= 2 \times \left[\int_{\frac{f_s}{4}-\frac{B}{2}}^{\frac{f_s}{4}+\frac{B}{2}} (2\cos 2\pi f T_s)^{2L} \cdot \frac{\Delta^2}{12} \cdot \frac{1}{f_s}\ df \right]$$

$$\approx \frac{\Delta^2}{12} \times \frac{\pi^{2L}}{2L+1} \times \frac{1}{M^{2L+1}} \tag{3.31}$$

where M is defined as $f_s/(2 \times B)$, with B being the width of the signal passband, as illustrated in Figure 3.13.

In cases where the signal passband is centered at an intermediate frequency, it is not strictly correct to refer to M as the oversampling ratio. The oversampling ratio is defined as the ratio of the actual sampling frequency to the minimum sampling frequency that avoids destructive aliasing. For lowpass modulators, the signal bandwidth extends from dc to f_b; thus, the minimum sampling frequency that avoids destructive aliasing is $2 \times f_b$, which is commonly referred to as the Nyquist rate. Therefore, the oversampling ratio for a lowpass modulator is equal to the sampling frequency divided by the Nyquist rate, $f_s/(2 \times f_b)$. However, for bandpass signals, in which the signal passband has a bandwidth of B and is centered at an intermediate frequency, f_{IF}, the minimum sampling frequency required to avoid destructive aliasing is only approximately equal to $2 \times B$. The exact expression for the minimum sampling frequency is

$$f_{min} = \frac{2\left(f_{IF} + \frac{B}{2}\right)}{\left\lfloor \frac{f_{IF} + \frac{B}{2}}{B} \right\rfloor} \tag{3.32}$$

where $\lfloor x \rfloor$ is equal to the largest integer not exceeding x [59], [60]. Hence, the oversampling ratio in a bandpass system should be defined as f_s/f_{min} with f_{min} given by (3.32). Regardless, the convention in the literature for bandpass modulators is to refer to $f_s/(2 \times B)$ as the oversampling ratio in order to preserve the terminology from lowpass modulators. Thus, the expression for the inband noise power calculated in (3.31) takes on the same form as the expression derived for an L^{th}-order lowpass modulator, (3.17). The expression for the dynamic range of the canonical $2L^{th}$-order, $f_s/4$ modulator,

$$DR = \frac{\frac{1}{2}\left(\frac{\Delta}{2}\right)^2}{\frac{\Delta^2}{12} \times \frac{\pi^{2L}}{2L+1} \times \frac{1}{M^{2L+1}}} = \frac{3}{2} \times M^{2L+1} \times \frac{2L+1}{\pi^{2L}} \quad , \tag{3.33}$$

also corresponds to that of an L^{th}-order lowpass modulator, (3.18).

The expressions that have been derived for the inband noise power, (3.31), and dynamic range, (3.33), of a $2L^{th}$-order, $f_s/4$ modulator closely match the results of behavioral simulations of the modulator using MIDAS [61]. The following figures show results from these simulations. In the following discussion, the modulator's full-scale analog input range is defined as the step size of its single-bit quantizer, Δ. Thus, the 0 dB level corresponds to the power of a sinusoid with an amplitude of $\Delta/2$. Figure 3.16 shows the undecimated spectrum of the fourth-order, $f_s/4$ modulator of Figure 3.14 when a –10 dB input been applied. In Figure 3.17, the signal-to-noise ratio in a 200-kHz passband vs. input signal level is seen to closely correspond to the straight-line characteristic derived from a linearized model of the modulator. However, it is not evident from these figures that large families of out-of-band tones begin to emerge at dc and $f_s/2$ when the input signal level decreases below approximately –40 dB. An example of these tones is illustrated in Figure 3.18 for a –50 dB input signal. Under normal modulator operation, the existence of such tones would not be problematic because they are ostensibly rejected by the digital decimation filter. However, if distortion mechanisms are present in the analog implementation of the modulator, then out-of-band tones at dc and $f_s/4$ can mix with the input signal and fall into the passband centered at $f_s/4$. In Chapter 7, it is postulated that this type of

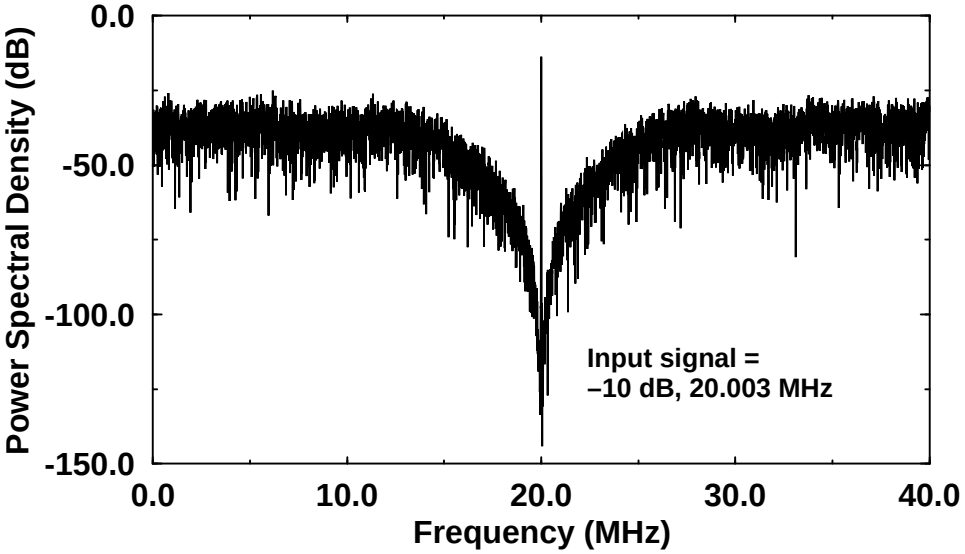


Figure 3.16: Undecimated spectrum of a canonical, fourth-order, $f_S/4$ modulator.

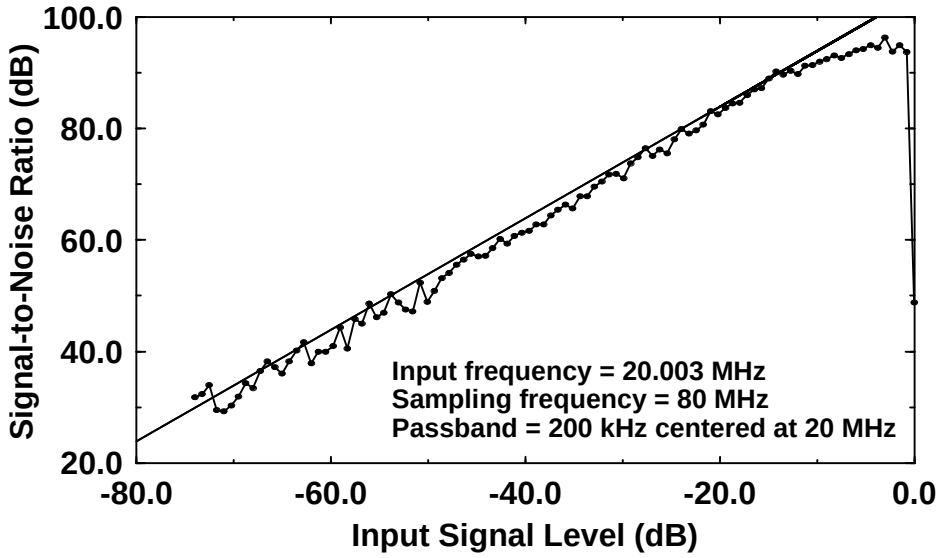


Figure 3.17: SNR vs. Input Signal Level of a canonical, fourth-order, $f_S/4$ modulator.

distortion is the mechanism that limits the performance of the experimental prototype described in this work. A thorough discussion of the measured data that supports this hypothesis is delayed until the experimental prototype is described in Chapter 7. It will

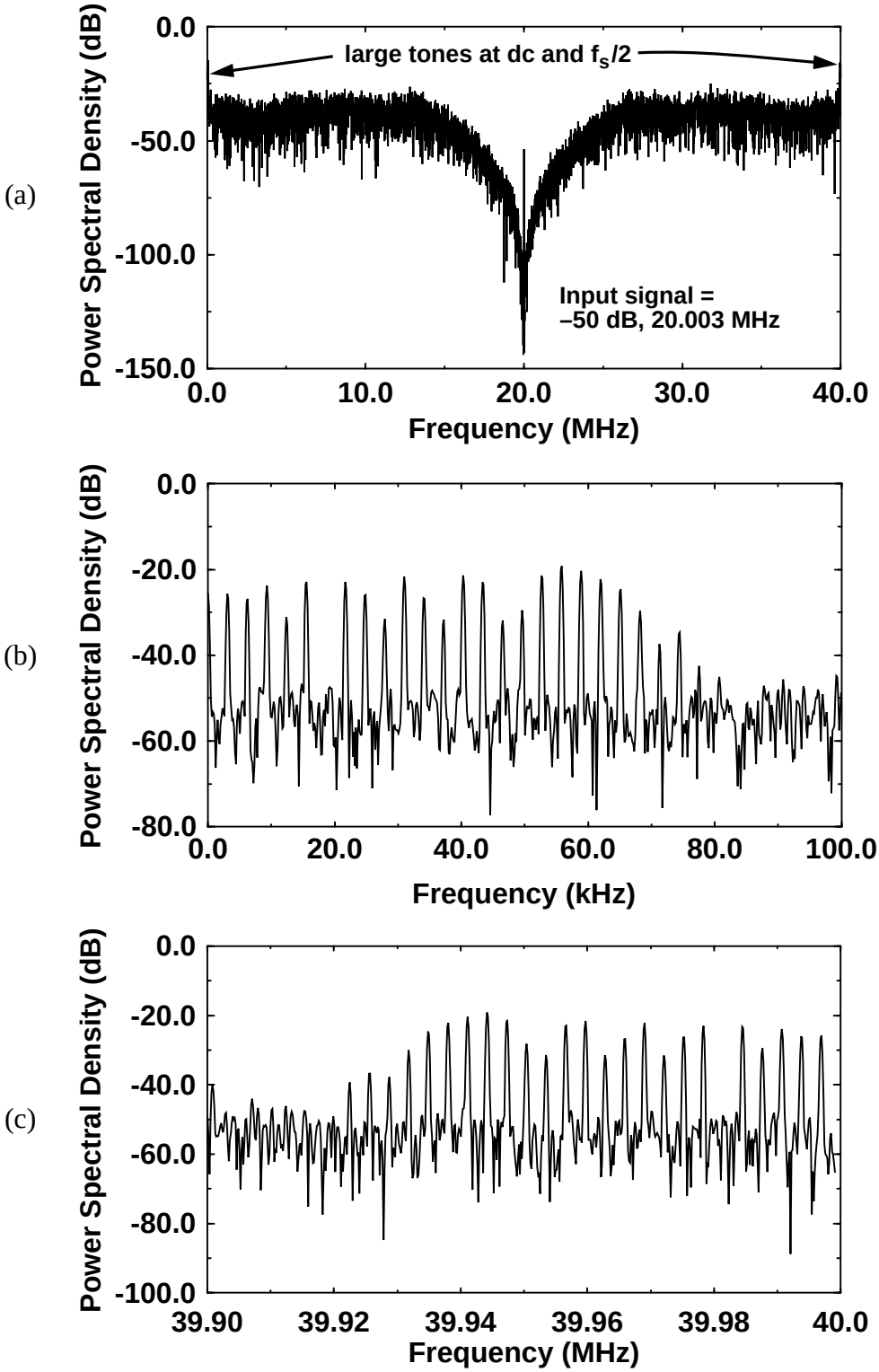


Figure 3.18: (a) Undecimated spectrum of a canonical, fourth-order, $f_s/4$ modulator. A close-in view around (b) dc and (c) $f_s/2$ (40 MHz).

also be shown in Chapter 7 that a small sinusoidal dither tone can suppress the generation of out-of-band tones.

The presence of out-of-band tones can also be attacked by modifying the architecture of the canonical $f_s/4$ modulator. Unfortunately, a general theory describing out-of-band tones and the conditions under which they can be suppressed has not yet been developed. Hence, tonal phenomena must be studied by means of extensive behavioral simulations. An initial exploration of different modulator architectures indicates that the tones can be suppressed by using a more complicated resonator topology than that depicted in Figure 3.14, or by designing the modulator architecture to center the signal passband away from $f_s/4$. The remainder of this chapter is devoted to an overview of these two speculative approaches.

3.3.3 $f_s/4$ Resonator Design Using a Continuous-time Prototype

The constituent resonators of a bandpass modulator can be designed by transforming an analog prototype resonator into a discrete-time, IIR filter through one of many different transformations between the continuous-time and discrete-time domains [18], [58]. In the following example, it is shown that if a fourth-order, $f_s/4$ modulator is implemented using resonators derived by means of the bilinear transform, the tones at dc and $f_s/2$ are substantially suppressed with respect to similar tones present in the output of the canonical, fourth-order, $f_s/4$ modulator for an equivalent input signal.

In the bilinear transform, the s-plane is mapped to one rotation around the unit circle in the z-domain via the transformation

$$s \rightarrow \frac{2}{T_d}\left(\frac{1-z^{-1}}{1+z^{-1}}\right). \tag{3.34}$$

The sampling parameter, T_d, is a carryover from the historical derivation of the bilinear transformation and can be arbitrarily chosen to be two with no loss in generality [18]. If $H_c(s)$ denotes the continuous-time prototype, then the corresponding discrete-time filter is

$$H_d(z) = H_c(s)\Big|_{s = \frac{1 - z^{-1}}{1 + z^{-1}}} . \tag{3.35}$$

The bilinear transformation is well-suited for the design of discrete-time resonators from continuous-time prototypes because there is no aliasing upon conversion from continuous-time to discrete-time. There is a one-to-one correspondence between the range of frequencies in the continuous-time domain, $-\infty < \omega_a < -\infty$, to those in the discrete-time domain, $-\pi < \omega_d < \pi$, through the nonlinear mapping

$$\omega_d = 2 \times \operatorname{atan} \omega_a . \tag{3.36}$$

A discrete-time resonator with a center frequency of $f_s/4$ ($\pi/2$ on a normalized discrete-time frequency axis), can be designed by applying the bilinear transform to the second-order, continuous-time resonator,

$$H_c(s) = \frac{1}{s^2 + \omega_o^2} , \tag{3.37}$$

which has a center frequency of ω_o. The resonant peak of the discrete-time filter is forced to lie at $f_s/4$ by prewarping the frequency response of the analog prototype according to (3.36). Thus, if the peak of $H_d(z)$ is to lie at $\pi/2$ (which corresponds to $f_s/4$), then the resonant frequency of the analog prototype, ω_o, must be tan ($\pi/4$), or 1. The resulting discrete-time bandpass resonator has the transfer function

$$H_d(z) = \frac{1}{s^2 + 1}\Bigg|_{s = \frac{1 - z^{-1}}{1 + z^{-1}}} = \frac{1}{2} \cdot \frac{(1 + z^{-1})^2}{1 + z^{-2}} . \tag{3.38}$$

At this point, the design of the discrete-time $f_s/4$ resonator is not yet complete. The resonator must include at least one delay in every branch; otherwise, the resulting modulator cannot be implemented because the loop around the quantizer will be delay free. Furthermore, behavioral simulations show that the stability of a bandpass modulator is affected by the phase response of the resonators in the region close to the resonant frequency. In this

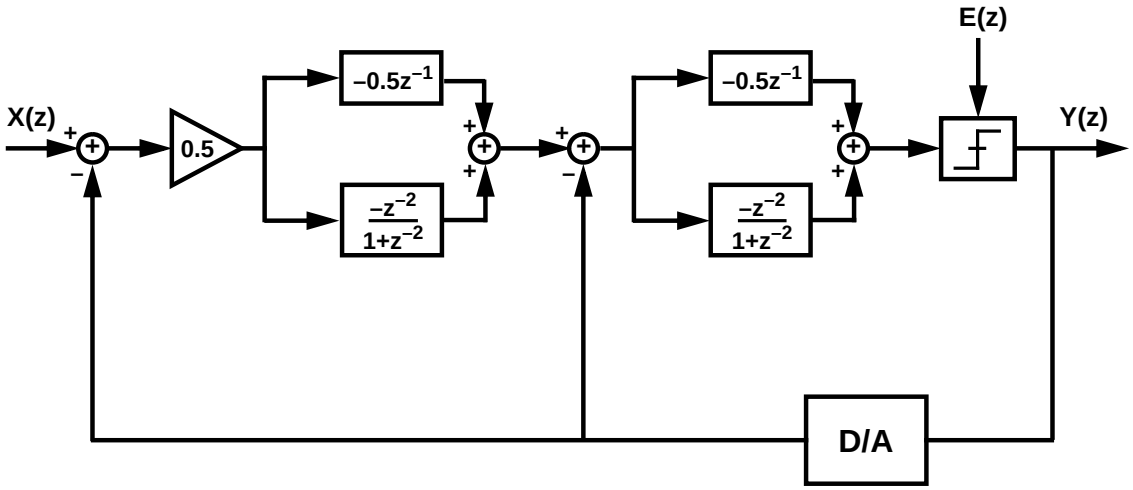


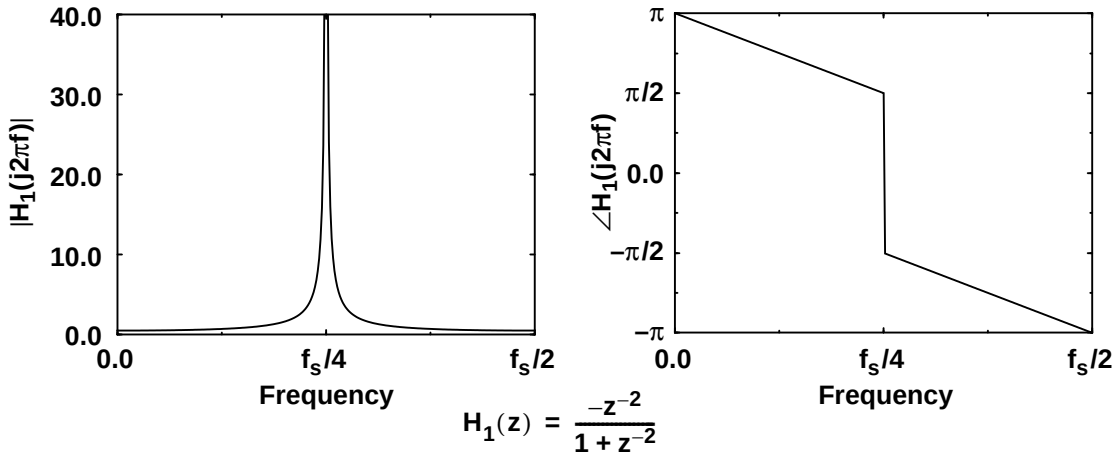
Figure 3.20: Fourth-order, $f_s/4$ modulator implemented with resonators designed using the bilinear transform.

example, it is possible to insure that every branch of the discrete-time $f_s/4$ resonator includes at least one delay by multiplying $H_d(z)$ by $-z^{-1}$. This also fortuitously insures that the phase response of the resulting resonator,

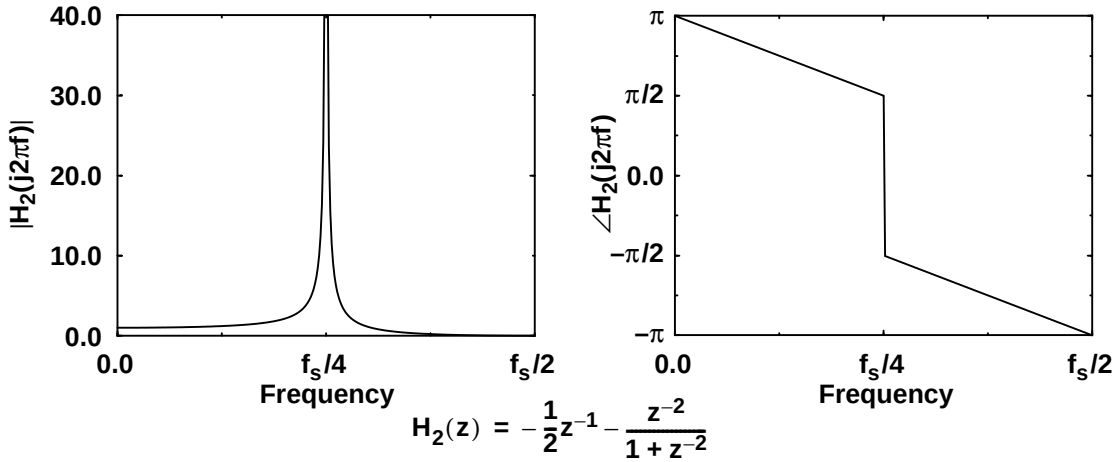
$$H_{res}(z) = -z^{-1}H_d(z) = -\frac{1}{2}z^{-1} - \frac{z^{-2}}{1+z^{-2}} \tag{3.39}$$

matches the phase response of the discrete-time $f_s/4$ resonator, (3.24), that was derived from a lowpass integrator by means of the dc-to-$f_s/4$ transformation, (3.23). The magnitude and phase responses of both $f_s/4$ resonators, (3.24) and (3.39), is shown in Figure 3.19.

Figure 3.20 depicts a fourth-order, $f_s/4$ modulator that is implemented using resonators with the transfer function of (3.39). In Figure 3.21, the tones at dc and $f_s/2$ for this architecture are compared with the similar tones present in the canonical, fourth-order, $f_s/4$ modulator. In comparison with Figure 3.20, the tones in the canonical modulator are seen to be approximately 10 dB to 20 dB higher for an equivalent input signal.



(a)



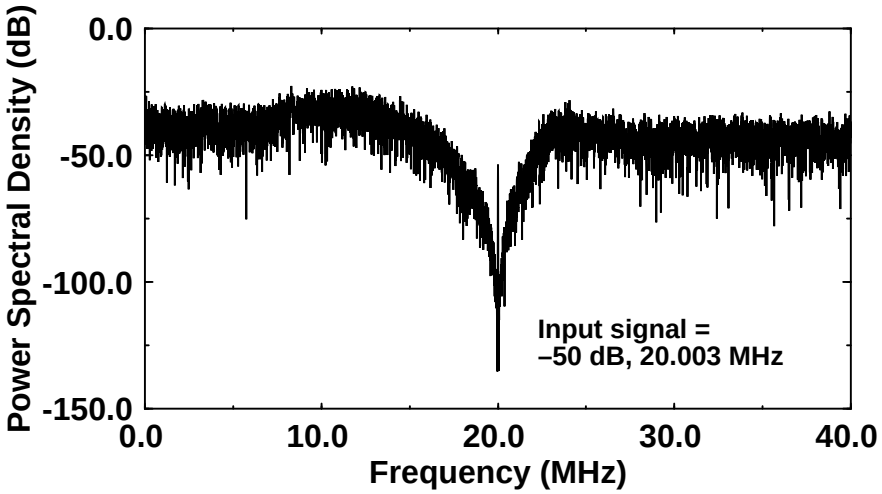
(b)

Figure 3.19: Magnitude and phase responses of a second-order, $f_S/4$ resonator with the transfer function, (a) $H_1(z)$, (3.24), and (b) $H_2(z)$, (3.39).

3.3.4 Generalized f_S/X Noiseshaping

The discussion of bandpass noiseshaping has so far been concerned primarily with modulator architectures that center the zeros of the noise transfer function at $f_S/4$. However, this may be unnecessarily restrictive from both a system-level perspective and a circuit imple-

(a)



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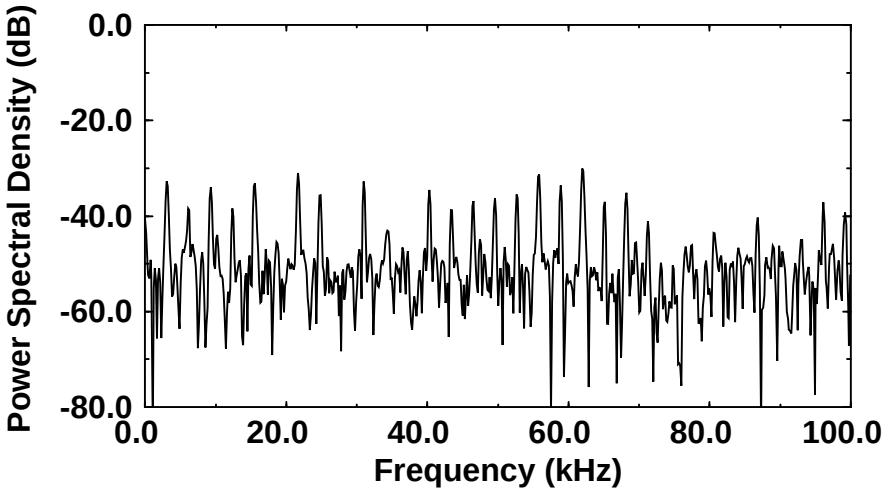

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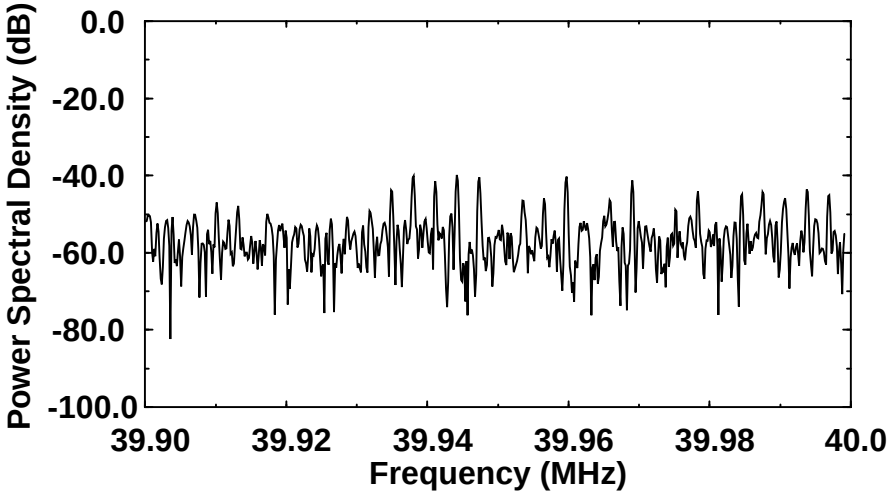


Figure 3.21: (a) Undecimated spectrum of an $f_S/4$ modulator with resonators derived from the bilinear transform. A close-in view around (b) dc and (c) $f_S/2$.

mentation standpoint. Two primary considerations motivate relocating the signal passband to a generalized location at f_s/X, where $2 < X < \infty$. First, when the passband is centered away from $f_s/4$, any distortion products resulting from the mixing of tones at $f_s/2$ with the input signal will fall outside the passband. Therefore, concern over out-of-band tones is partially relieved. Second, if the passband center frequency is situated between $f_s/4$ and $f_s/2$, the ratio of the modulator's sampling frequency to its passband center frequency is reduced. Therefore, if the modulator is implemented with a single-path topology, the demands upon the analog circuitry will be relaxed when the sampling rate is reduced. However, it should be noted that once the passband is centered away from $f_s/4$, the resulting modulator may not be suitable for implementation using the type of two-path architecture that is advantageous for modulators operating at high sampling speeds. This two-path architecture is developed in detail in Chapters 4 and 5.

The zeros of the noise transfer function can be positioned anywhere between dc and $f_s/2$ by generalizing the dc-to-$f_s/4$ transformation, (3.23), to allow the constituent resonators to realize their nominally infinite gain in a passband that is centered at any arbitrary frequency, f_s/X. If this transformation process yields a modulator architecture with undesirable characteristics, such as poor stability or overload recovery, then an alternative direct synthesis method may be employed. In this approach, the architecture of the bandpass modulator is designed to implement the desired noiseshaping function without relying on a transformation from the lowpass domain. The remainder of this chapter is devoted to a discussion of these two design procedures. It should be emphasized that the methodologies to be presented are neither complete nor proven to be optimal. In fact, in the absence of definitive theoretical analyses, extensive behavioral simulations of modulator architectures and empirical evidence in the open literature are offered as the only justification for the guidelines stated.

3.3.4.1 Constantinides Lowpass-to-Bandpass Transformation

Intuitively, if the integrators of the L^{th}-order, lowpass modulator depicted in Figure 3.11 are replaced by resonators that peak at f_s/X, then quantization noise will be suppressed in a

narrowband region centered around this resonant frequency. Therefore, architectures of f_s/X modulators can be derived by applying the appropriate transformation to the discrete-time integrators of an L^{th}-order, lowpass modulator. One robust transformation, (3.23), that results in $f_s/4$ modulators has already been described. A more general transformation due to Constantinides can be used to design modulator architectures with a signal passband centered anywhere between dc and $f_s/2$ [62].

As described by Constantinides, a discrete-time lowpass filter with cutoff frequency Ω_c can be transformed into a bandpass filter with lower and upper cutoff frequencies, ω_{c1} and ω_{c2} respectively, by means of the following algebraic z-variable substitution [18],

$$z^{-1} \rightarrow \frac{-z^{-2} + \frac{2\alpha k}{k+1} z^{-1} - \frac{k-1}{k+1}}{\frac{k-1}{k+1} z^{-2} - \frac{2\alpha k}{k+1} z^{-1} + 1} \quad . \tag{3.40}$$

In this expression, α and k are passband scaling parameters, and are given by

$$\alpha = \frac{\cos\left(\frac{\omega_{c2} + \omega_{c1}}{2}\right)}{\cos\left(\frac{\omega_{c2} - \omega_{c1}}{2}\right)} \tag{3.41}$$

and

$$k = \cot\left(\frac{\omega_{c2} - \omega_{c1}}{2}\right) \tan\left(\frac{\Omega_c}{2}\right) \quad . \tag{3.42}$$

The frequency variables in this transformation, ω_{c1}, ω_{c2}, and Ω_c, are all normalized such that dc to $f_s/2$ corresponds to 0 to π. Insofar as this transformation is expressly used to derive a resonator from a lowpass integrator, it is permissible to simplify expressions (3.40), (3.41), and (3.42) in the following manner. First, the lower and upper cutoff frequencies, ω_{c1} and ω_{c2}, are defined in terms of a center frequency, ω_o, and a deviation parameter, Δ, such that $\omega_{c1} = \omega_o - \Delta$, and $\omega_{c2} = \omega_o + \Delta$. Second, the deviation parameter,

Δ, is chosen to be zero such that ω_{c1} and ω_{c2} are equal to the desired resonator center frequency, ω_o. Thus, the scaling parameter, α, becomes

$$\alpha = \cos\omega_o \quad . \tag{3.43}$$

Finally, since the lowpass prototype filter is a discrete-time integrator with a magnitude response that has an infinite peak at dc, its –3-dB frequency is poorly defined. Therefore, the cutoff frequency, Ω_c, of the lowpass prototype can be arbitrarily chosen to equal 2Δ in order to streamline (3.40) by forcing $k = 1$. The Constantinides lowpass-to-bandpass transformation for resonators can then be written as

$$z^{-1} \rightarrow \frac{-z^{-2} + \cos\omega_o z^{-1}}{-\cos\omega_o z^{-1} + 1} \quad . \tag{3.44}$$

For $\omega_o = \pi/2$, which corresponds to $f_s/4$, (3.44) collapses to the previously described transformation, $z^{-1} \rightarrow -z^{-2}$.

Under (3.44), a discrete-time lowpass integrator is transformed into a bandpass resonator with the transfer function,

$$H_{bp}(z) = \left.\frac{z_{lp}^{-1}}{1 - z_{lp}^{-1}}\right|_{z_{lp}^{-1} = \frac{-z^{-2} + \cos\omega_o z^{-1}}{-\cos\omega_o z^{-1} + 1}} = \frac{\cos\omega_o z^{-1} - z^{-2}}{1 - 2\cos\omega_o z^{-1} + z^{-2}} \quad . \tag{3.45}$$

One possible z-domain implementation of this resonator is shown in Figure 3.22 [63].

A fourth-order, $f_s/6$ modulator can now be designed by applying transformation (3.44) to the integrators in the canonical, second-order lowpass prototype of Figure 3.9. For example, if $\omega_o = \pi/3$, then the $f_s/6$ modulator shown in Figure 3.23 results. The simulated undecimated spectra of this architecture, presented in Figure 3.24, show that the noise is indeed suppressed in a narrowband region around $f_s/6$. Furthermore, it is noteworthy that the region around dc appears to be free of spurious tones for the –50 dB input signal shown.

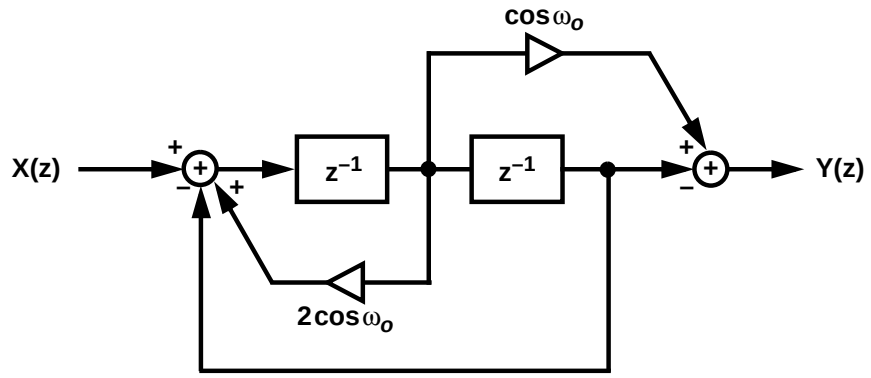


Figure 3.22: A possible *z*-domain implementation of a generalized ω_o resonator with the transfer function (3.45).

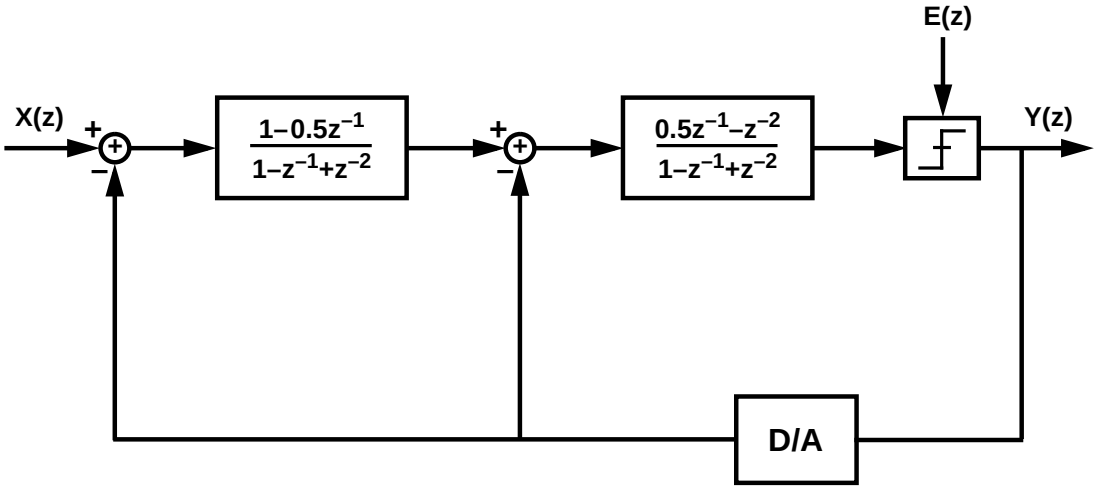


Figure 3.23: Fourth-order, $f_S/6$ modulator implemented with resonators designed using the Constantinides transform.

3.3.4.2 Direct Synthesis of the Noise Transfer Function

It has been shown that fourth-order, f_S/X modulators can be designed by operating on a lowpass prototype with one of several transformations. However, only a limited class of bandpass architectures can be derived in this manner. If more degrees of freedom for

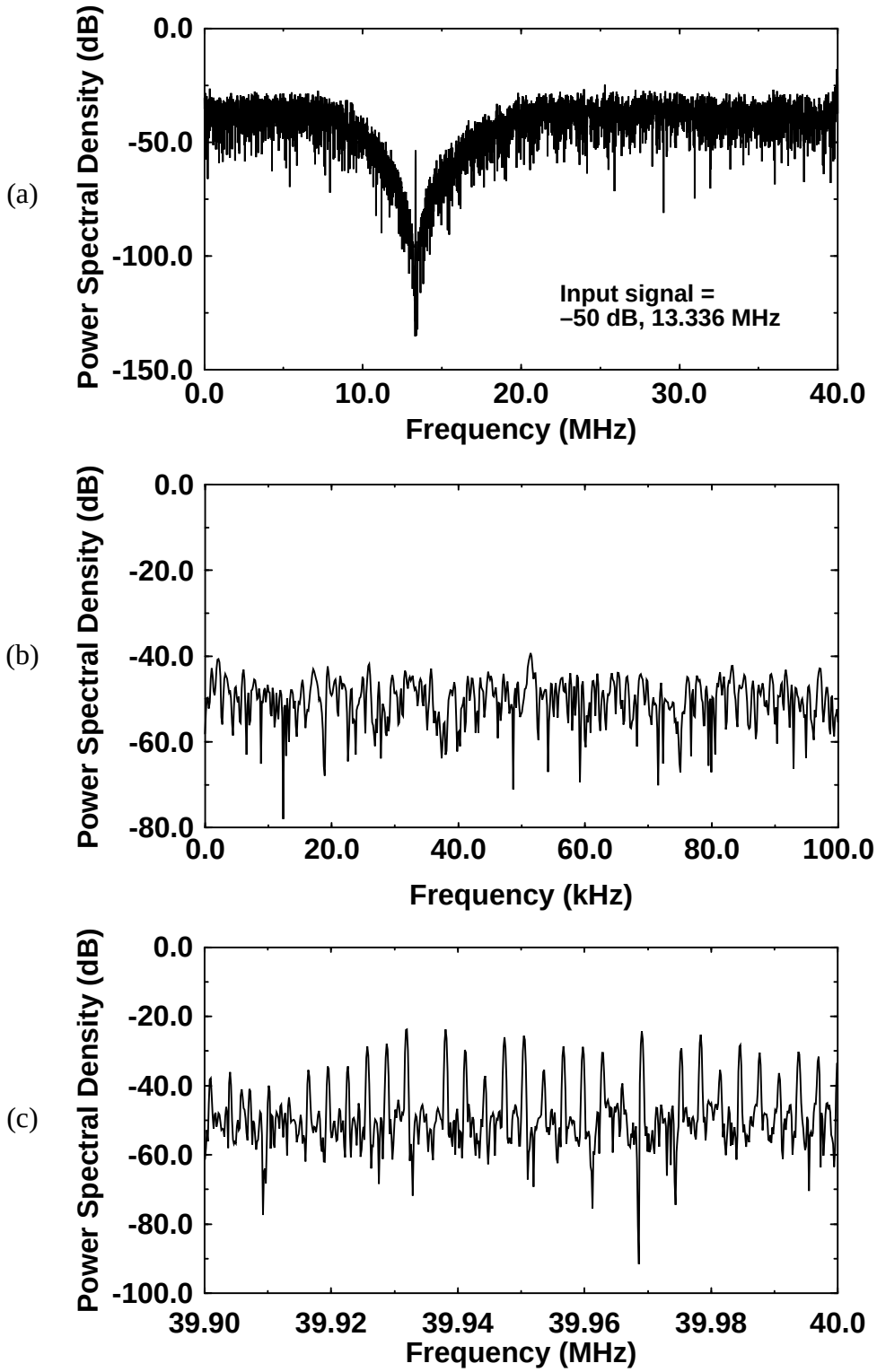


Figure 3.24: Undecimated output spectrum of an $f_S/6$ modulator with resonators derived from Constantinides transform. A close-in view around (b) dc and (c) $f_S/2$.

architectural optimization, or higher-order ($2L > 4$) noiseshaping in a single-loop topology are desired, then the design process must be focused specifically on the noise transfer function (NTF) of the modulator. From this perspective, the modulator design process is essentially reduced to one of filter design; once a suitable NTF has been identified, an architecture that implements this transfer function is synthesized.

Architectures derived by direct synthesis of the noise transfer function offer more flexibility than those derived by transforming a lowpass prototype because the modulator can be tuned with respect to specific performance metrics by manipulating the NTF. For example, behavioral simulations show that the peak signal-to-quantization noise ratio near overload is correlated with the out-of-band gain of $NTF(z)$. Therefore, if the peak SNR is not sufficient, the NTF can be redesigned to have a larger out-of-band gain. This design procedure opens the possibility of using computer-aided optimization tools to design an $NTF(z)$ that maximally suppresses the inband quantization noise with respect to a specified cost function [64]. In practice, however, this degree of optimization may not be worthwhile because the minimum detectable signal in efficient implementations of modulators is virtually always determined by circuit, rather than quantization, noise.

The direct synthesis of a bandpass noiseshaping modulator is similar in many ways to the design of higher-order, single-loop, lowpass modulators, which are comprised of multiple (> 2) integrators embedded in a feedback topology. In both domains, lowpass as well as bandpass, the design of the modulator begins with identifying a noise transfer function that adheres to certain empirically derived criteria [45]-[47]. The concern is that the presence of multiple poles enclosed within a feedback loop will induce an instability in the modulator. In this context, instability refers to the condition in which the internal states of the modulator exhibit large, and possibly unbounded, excursions that persist even after the input signal is removed. In addition, during overload or instability, the signal-to-noise ratio at the output of the modulator will be substantially below that predicted by a linearized, stochastic model of the system. The design goal is to inhibit this potential instability by imposing restrictions on the shape and out-of-band gain of $NTF(z)$, while insuring that such constraints are not so severe as to compromise the inband noise suppression.

Once the noise transfer function has been identified, a feedback modulator that shapes the quantization noise with the desired NTF can be designed. In Figure 3.7, the filter in the forward path of the modulator, $A(z)$, can be found from algebraic manipulations of $NTF(z)$. If the feedback filter, $F(z)$, is assumed to be 1, $A(z)$ is easily found to be

$$A(z) = \frac{1}{NTF(z)} - 1 \quad . \tag{3.46}$$

The physical implementation of the modulator imposes a causality restriction on $A(z)$. Because the feedback filter, $F(z)$ is assumed to be 1, the forward path filter cannot contain any delay-free branches; otherwise, when $A(z)$ is embedded in the modulator, the loop around the quantizer will not include any delays. This implies that any change at the input to the modulator will manifest itself immediately at the output and propagate through the feedback D/A converters back to the input in the same clock phase, thus contradicting the clocked nature of the circuit implementation.

The forward path filter can be written in the following general form

$$A(z) = \frac{b_1 z^{-1} + b_2 z^{-2} + \ldots + b_N z^{-N}}{a_o + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_N z^{-N}} \quad . \tag{3.47}$$

Therefore, it can be seen that the requirement for a minimum delay of z^{-1} in $A(z)$ can be equivalently stated as the following constraint on $NTF(z)$,

$$\lim_{z \to \infty} NTF(z) = 1 \quad . \tag{3.48}$$

Stability imposes the second primary constraint on the noise transfer function. Extensive simulations of fourth-order noiseshaping modulators, both lowpass and bandpass, indicate that the stability of the system is correlated with the out-of-band gain of $NTF(z)$. In particular, it is desirable to constrain the out-of-band gain such that

$$|NTF(z)| < 2 \tag{3.49}$$

for all z such that $|z| = 1$ [45]-[47]. For some classes of modulators, this bound can be violated by a large margin without any apparent impact on the stability of the system. However, in general, behavioral simulations confirm a correlation between (3.49) and the stability of the modulator. Also, the shape of $|NTF(z)|$ should be relatively "smooth" and should not contain any unusual resonances [46]. Unfortunately, theoretical justifications for these criteria remain poorly developed and are often of questionable merit since they tend to be based upon the profoundly weak premise that the modulator can be modeled as a linear stochastic system. Also, it should be noted that (3.49) pertains only to fourth-order noise transfer functions. Higher-order transfer functions, which correspond to more aggressive noiseshaping, may be constrained by a smaller bound. Nevertheless, insofar as these facts are recognized, (3.49) is useful in guiding the initial development of a fourth-order, f_s/X bandpass modulator. Due to the speculative nature of (3.49), more conservative bounds, such as 1.5, are often advocated in the interests of improving the safety margin with respect to instability [46], [47].

One practical step-by-step design flow that has already be described for the design of higher-order lowpass modulators [47] can be adapted for the design of $2L^{th}$-order, f_s/X modulators:

(1) Design a $2L^{th}$-order noise transfer function. Position the zeros of the NTF at f_s/X, and insure that the NTF satisfies the criteria for causality, (3.48), as well as the bound on out-of-band gain, (3.49). The NTF can be designed using any of several discrete-time filter synthesis techniques that yield approximations to common continuous-time filter families such as Butterworth, Chebyshev, or elliptical. Or, the NTF can be designed using an IIR filter synthesis tool such as the *yulewalk* function in MATLAB that converges upon a transfer function when the desired frequency response and filter order are specified.

The inexact nature of a VLSI implementation of the modulator can motivate the choice of filter family. For example, the zeros of a Butterworth noise transfer function lie coincident upon one another at the center of the passband. Therefore, the frequency response of Butterworth NTFs in the vicinity of the passband is largely unaffected

when the coefficients of the transfer function are modestly perturbed, as will be the case in any analog implementation of the modulator.

(2) Design a modulator that implements the NTF found in step 1, and simulate it using MIDAS or some other behavioral simulator. One possible modulator topology that can be easily mapped to a VLSI implementation employs a cascade of second-order resonators and is described at the end of this section.

(3) If the modulator is unstable, reduce the out-of-band gain of the noise transfer function.

(4) If the modulator is stable, but the peak SNR of the output is not sufficient, increase the out-of-band gain of the noise transfer function.

(5) Perturb the filter coefficients of the modulator and resimulate the architecture to insure that its performance is largely insensitive to the exact values of the path filters.

(6) Determine the recovery characteristics of the modulator by briefly overdriving the input and then reducing the input signal level. The internal states of the modulator should not continue to increase without bound once the input signal has been reduced below the 0 dB level. The modulator should also be tested by preloading the internal states with an overload condition. When an input signal below 0 dB is applied, the internal states should subside to a level consistent with normal modulator operation. If the modulator does not recover under these conditions, a state variable reset must be incorporated into the design of the modulator. Clamping circuits at the inputs to each operational amplifier may be required as well [65].

Appendix A illustrates this design flow more explicitly by describing the design of a fourth-order, $f_s/6$ modulator.

The forward path filter, $A(z)$, can be implemented using many different z-domain topologies, but from a practical perspective, if the topology is comprised of cascaded, second-order sections, it can be mapped easily to a VLSI implementation based upon standard second-order biquadratic filters.

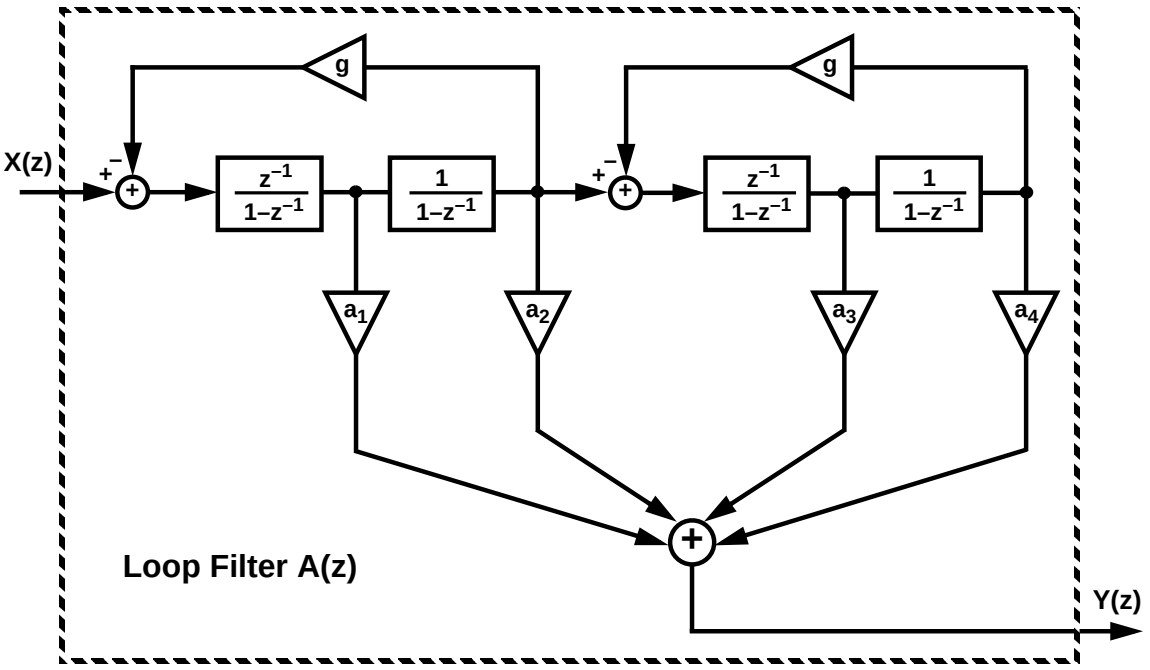


Figure 3.25: Implementation of the forward path filter, $A(z)$, using a cascade of resonators.

One possible implementation using a cascade of resonators with feedforward branches is illustrated in Figure 3.25. The transfer function of the filter can be written in terms of the feedback and feedforward gains as

$$A(z) = \frac{(a_1 + a_2)z^{-1} + (-3a_1 - 2a_2 + a_3 + a_4 + g(a_1 + a_2))z^{-2}}{(1-(2-g)z^{-1} + z^{-2})^2} + \frac{(3a_1 + a_2 - a_3 + a_1 g)z^{-3} - a_1 z^{-4}}{(1-(2-g)z^{-1} + z^{-2})^2} \quad . \tag{3.50}$$

The center frequency, ω_{res}, of $A(z)$ is determined by the poles of (3.50), and they are situated at

$$\omega_{res} = \pm \text{acos}\left(1 - \frac{g}{2}\right) \quad . \tag{3.51}$$

With five degrees of freedom, a_1 to a_4, and g, the cascade-of-resonators structure can be used to synthesize any fourth-order transfer function with poles coincident at $\pm\omega_{res}$, and the structure can be generalized in straightforward manner to implement a $2L^{th}$-order transfer function. In addition, through the use of different feedback gains, g_1 and g_2, the poles of $A(z)$ can be distributed within the signal passband rather than forcing them to be coincident at the passband center frequency, $\pm\omega_{res}$. This may be necessary if the oversampling ratio is low and the quantization noise must be suppressed in a wide signal bandwidth.

3.4 Summary

The design of high-resolution, Nyquist-rate A/D converters in a modern submicron technology is limited by device matching and the need to implement a precise antialiasing filter with a narrow and well-defined transition band. These limitations can be circumvented by utilizing oversampling and feedback to shape the quantization noise away from a narrow passband.

Traditionally, feedback modulators have been developed on the premise that quantization noise is to be suppressed in a region centered at dc. However, by replacing the constituent integrators of a lowpass modulator with resonators that realize an infinite gain at f_s/X, it is possible to suppress quantization noise in any portion of the spectrum from dc to $f_s/2$. Special design procedures must be followed in order to insure the stability of the resulting bandpass noiseshaper. The bandpass architecture can be designed by applying different lowpass-to-bandpass transformations to a lowpass prototype, or the modulator can be designed to directly implement a specific noiseshaping function without relying on a transformation from the lowpass domain.

The choice of architecture for a bandpass modulator is motivated by various design criteria. For example, system-level characteristics such as overload recovery, signal excursions at internal nodes, and out-of-band spectral coloration, are fundamentally impacted by changes in the modulator architecture. In fact, behavioral simulations indicate that if

the signal passband is centered away from $f_s/4$, the output spectrum of the modulator will not contain strong tones at dc for low-level input signals. However, the attendant increase in circuit complexity required to implement a generalized cascade-of-resonators modulator topology may preclude the use of a non-$f_s/4$ architecture at sampling rates of tens of MHz. These system- and circuit-level issues are explored further in the following chapter when the design of a fourth-order, $f_s/4$ modulator intended to digitize signal passbands centered as high as 20 MHz is described.

Chapter

4

Design of a Fourth-Order, $f_s/4$ Modulator

A number of experimental modulators based upon the bandpass architectures discussed in the previous chapter have been reported for a variety of applications requiring the IF digitization [50], [55], [56], [66]-[71] of narrowband (< 200 KHz) passbands. However, in many of these modulators, those that achieve a dynamic range suitable for wireless systems (> 70 dB) have also been limited to digitizing passbands centered at relatively low intermediate frequencies of under 5 MHz [55], [69]. This limitation is due in part to the fact that these modulators utilize an $f_s/4$ architecture, which means that the modulator must sample the input signal at a rate equal to four times the passband center frequency. Therefore, with an IF of 5 MHz, the modulator sampling rate must already be 20 MHz. At this frequency, the achievable dynamic range of the modulator can be influenced significantly by analog circuit nonidealities such as incomplete and nonlinear settling of the amplifier outputs. Extrapolating to the higher sampling rates necessary to digitize IF signals centered above 10 MHz, the performance of the modulator may be compromised to such a degree that it is no longer viable for the intended application. This limits the utility of bandpass modulators for wireless IF digitization because in receivers for RF carriers between 1 and 2 GHz, a second IF location between 10 and 20 MHz is typically chosen to meet the competing requirements for image rejection and channel selectivity [72].

This chapter discusses the system-level design and analog circuit requirements for a fourth-order, $f_s/4$ modulator that digitizes a signal passband centered as high as 20 MHz.

Potential system-level problems such as large internal signal swings, offset, and timing jitter are identified and analyzed. Following the discussion of the system architecture, the primary circuit-level imperfections that impair the modulator at high sampling speeds are considered. The impact of these circuit-related limitations is analyzed by considering their effect on switched-capacitor biquadratic filters, which are the conventional building blocks for discrete-time bandpass modulators. The penalty in the modulator's dynamic range is assessed by means of a behavioral model of the modulator that includes circuit nonidealities. It is suggested that the demands imposed on the analog circuitry can be reduced by a factor of two by implementing the modulator using a two-path topology.

4.1 System Design of an $f_s/4$ Modulator Architecture

In this work, canonical $f_s/4$ bandpass topologies that are derived using the dc-to-$f_s/4$ transformation, (3.23), are the topologies of choice for high-speed modulator designs because these topologies can be implemented using comparatively simple circuit structures. More specifically, $f_s/4$ topologies derived using (3.23) can be implemented using two-path filters. A thorough discussion of the two-path design issues is delayed until the following chapter, but it can be stated briefly that the main motivation for using a two-path topology is that the path filters are clocked at only one-half of the effective sampling frequency of the modulator. Therefore, for a given sampling frequency, the allowable settling time for each analog block is increased by a factor of two. In this manner, the time allotted for settling in the analog circuitry can be increased by a greater margin than by placing the signal passband closer to $f_s/2$ and operating the modulator at a lower sampling frequency. The remainder of this chapter is devoted to a discussion of the system-level modulator design and an analysis of the analog circuit nonidealities that motivate the use of a two-path topology.

4.1.1 Modifications to the Canonical $f_s/4$ Topology

If the dc-to-$f_s/4$ transformation, (3.23), is applied to the second-order lowpass prototype of Figure 3.9, the canonical, fourth-order, $f_s/4$ topology depicted in Figure 3.14 is obtained. This topology is referred to as being canonical because it is derived directly from the original, second-order topology described by Candy for lowpass noiseshaping [13]. Owing to this lineage, it is not surprising to note several common limiting factors between both topologies.

The first limitation arises from the fact that there is a non-delaying filter in the forward path of both modulators. In general, it is not desirable to implement a non-delaying, sampled-data analog filter because of the implicit need to sample the output of the filter during the same clock phase that an input stimulus is causing charge to flow between capacitors [73]. In such a situation, the operational amplifier is directly involved in the sampling process, which implies that the final value of the output sample will exhibit an increased dependency on the settling behavior of the amplifier. For example, an abrupt change at the input may induce nonlinear, slew-limited amplifier settling, which is then manifested immediately at the output. These adverse effects become especially acute when a signal must propagate through more than one unsettled operational amplifier, which is the case in a biquadratic implementation of the non-delaying, second-order resonator in the canonical $f_s/4$ modulator. To circumvent this limitation, input and output sampling can be decoupled by phasing the switches of the switched-capacitor filter to introduce a half- or full-sample delay between the input and output.

A second limitation common to both lowpass and bandpass modulator topologies is that the internal signal excursions within the modulators can be several times larger than the range of the quantizer output, $\pm\Delta/2$. In the following discussion, it is also useful to define $\pm\Delta/2$ as the full-scale analog input range, in which case, the 0 dB level corresponds to the power of a sinusoid with an amplitude of $\Delta/2$. The large signal swings at internal nodes impose a severe disadvantage in circuit technologies where the dynamic range of the system is constrained by a modest supply voltage. For example, in submicron CMOS

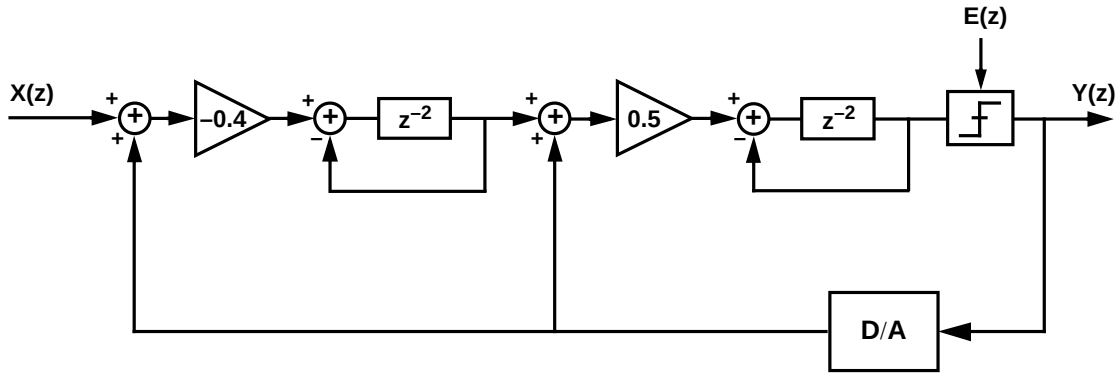


Figure 4.1: Proposed $f_s/4$ modulator topology with internal signal scaling and delays in the forward path of both resonators.

technologies, the supply voltage is often limited to 3.3 V or less. Fortunately, the range of the internal signal excursions can be limited by scaling the system gains of the modulator architecture appropriately.

The disadvantages associated with non-delaying filters and wide signal excursions at internal nodes have been well documented for lowpass modulators, and a modified topology for lowpass modulators that circumvents these limitations has been proposed by Boser [14]. The Boser lowpass topology was adapted by Song for $f_s/4$ noiseshaping by applying the dc-to-$f_s/4$ transformation, (3.23) [56]. The Song $f_s/4$ topology forms the basis of the experimental $f_s/4$ modulator implemented in the course of this research and described in this dissertation.

In the proposed $f_s/4$ topology depicted in Figure 4.1, both forward path resonators include a delay of z^{-2}, and the system gains of the resonators have been scaled to reduce the signal excursions at the outputs of the two resonators. The signs of the system gains are determined by the dc-to-$f_s/4$ transformation, (3.23). The system gain of the first resonator, –0.4, was chosen on the basis of behavioral simulations of the signal-to-quantization noise ratio for a –2 dB input signal as the value of the first resonator gain was swept from –2.0 to 0. As seen in Figure 4.2, with an 80 MHz sampling frequency and a 20.003 MHz, –2 dB input signal, the peak signal-to-quantization noise ratio is obtained with a gain of

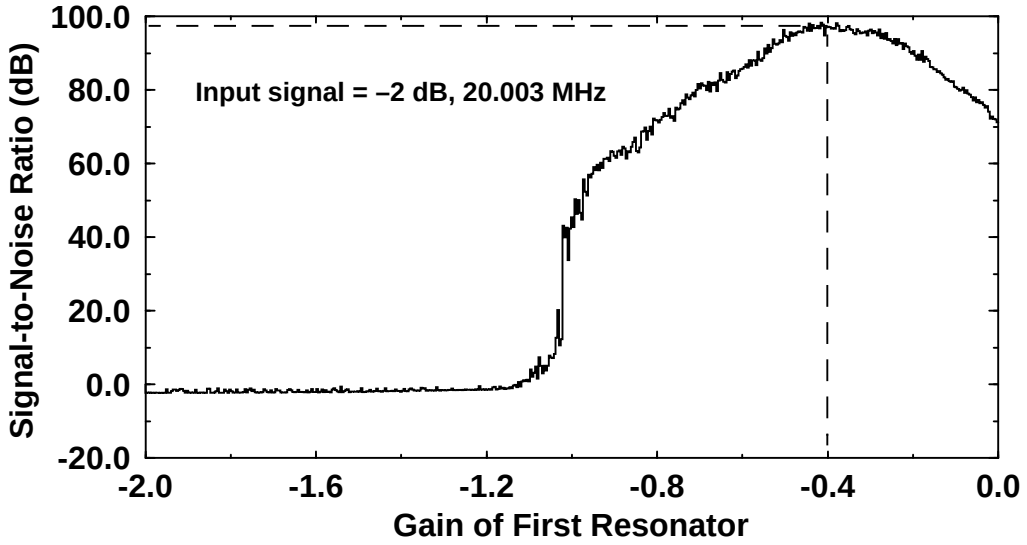


Figure 4.2: Simulated inband signal-to- noise ratio vs. the gain of the first resonator.

approximately –0.4 in the first resonator. The absolute value of the gain of the second resonator can be freely chosen because it is followed immediately by a single-bit quantizer. Therefore, based on signal-swing considerations, the gain of the second resonator was set to 0.5. A comparison of the internal signal swings in the proposed $f_s/4$ topology with those in the canonical $f_s/4$ topology is shown in Figure 4.3. In the proposed topology, it is seen that the maximum signal excursion at the output of the first integrator is approximately equal to the magnitude of the feedback reference levels, $\Delta/2$.

4.1.2 Signal and Noise Transfer Functions

If the quantizer in Figure 4.1 is approximated as a gain, G_Q, with an additive, uncorrelated noise source, E(z), the output of the modulator is described in the z-domain by

$$Y(z) = \frac{-0.2G_Q \cdot z^{-4}X(z) + (1+z^{-2})^2 E(z)}{1 + (2 - 0.5G_Q) \cdot z^{-2} + (1 - 0.3G_Q) \cdot z^{-4}} \quad . \tag{4.1}$$

Behavioral simulations of the experimental modulator using MIDAS [61] indicate that the power of the quantization noise in the signal passband is accurately estimated from (4.1)

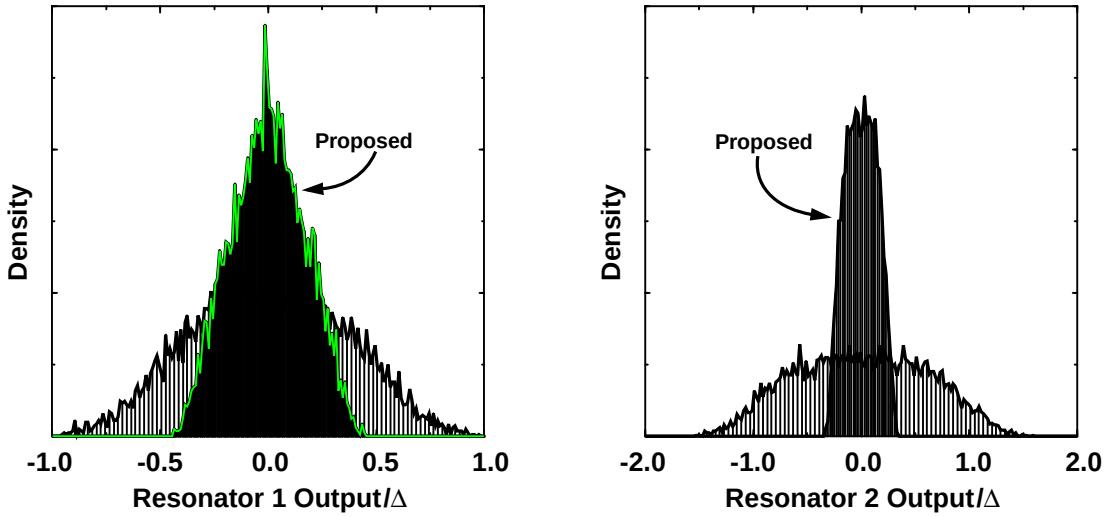


Figure 4.3: Comparison of signal swings at the outputs of the (a) first and (b) second resonators for the canonical $f_s/4$ modulator vs. the proposed $f_s/4$ modulator for an –10 dB input signal.

by setting the gain of the quantizer, G_Q, to 5. With $G_Q = 5$, the transfer function of the modulator, (4.1), can be simplified near $f_s/4$ by making the approximation $z \approx e^{j2\pi(f_s/4)T_s} = j$, which leads to

$$Y(z) \approx -z^{-4}X(z) + (1 + z^{-2})^2 E(z) \ . \tag{4.2}$$

Thus, the output of the modulator consists of the input, *X(z)*, delayed by four sample periods, together with a bandstop shaping of the additive quantizer noise, *E(z)*. As discussed in Chapter 3, it is important to note that the white noise model of the quantizer ignores the strong correlation between the quantization noise and the input that is inherent to any oversampling modulator employing a single-bit quantizer. This correlation results in spurious noise tones. One class of such tones at dc and $f_s/2$ was described in Chapter 3, and the impact of these tones on modulator performance is discussed in detail in Chapter 7, where measured results from the experimental prototype are presented.

4.1.3 Quantization and Electronic Noise Limitations

An efficient, practical implementation of the modulator depicted in Figure 4.1 will generally be limited by electronic noise rather than quantization noise. At the high sampling frequencies necessary to digitize a 200-kHz passband centered between 10 MHz and 20 MHz, the high oversampling ratio usually guarantees that the quantization noise floor is suppressed well below the electronic noise. In the case of the proposed fourth-order modulator, at a sampling frequency of 80 MHz, a 200-kHz signal passband centered at 20 MHz is digitized with an oversampling ratio of 200. For this oversampling ratio, behavioral simulations show that the inband quantization noise floor is approximately 95 dB below the full-scale input signal level, $\pm\Delta/2$. Because the quantization noise is attenuated by a large margin with respect to the anticipated level of electronic noise in the circuit, it can virtually be disregarded.

If the quantization noise is assumed to be negligible with respect to electronic noise, it can be shown that the noise sources at the front end of the modulator limit the achievable resolution of the system. Wideband noise injected at the inputs to the second resonator and the comparator are suppressed in the signal passband by second- and fourth-order noise transfer functions, respectively, but front-end noise is not spectrally shaped [14]. In a switched-capacitor implementation of the modulator, significant noise sources at the front end include thermal noise in the MOS switches, which results in kT/C noise being sampled onto capacitors, input-referred operational amplifier noise, and noise in the feedback D/A converters. In the experimental prototype, the total noise in the signal bandwidth is dominated by a combination of amplifier noise and kT/C noise and will be quantified in Chapter 6.

4.1.4 Offset

Offset in a bandpass $\Sigma\Delta$ modulator can be troublesome even though offset-related artifacts often lie outside the signal band [50]. The presence of high-level, out-of-band tones can compress the available dynamic range of the modulator; moreover, they can mix into the

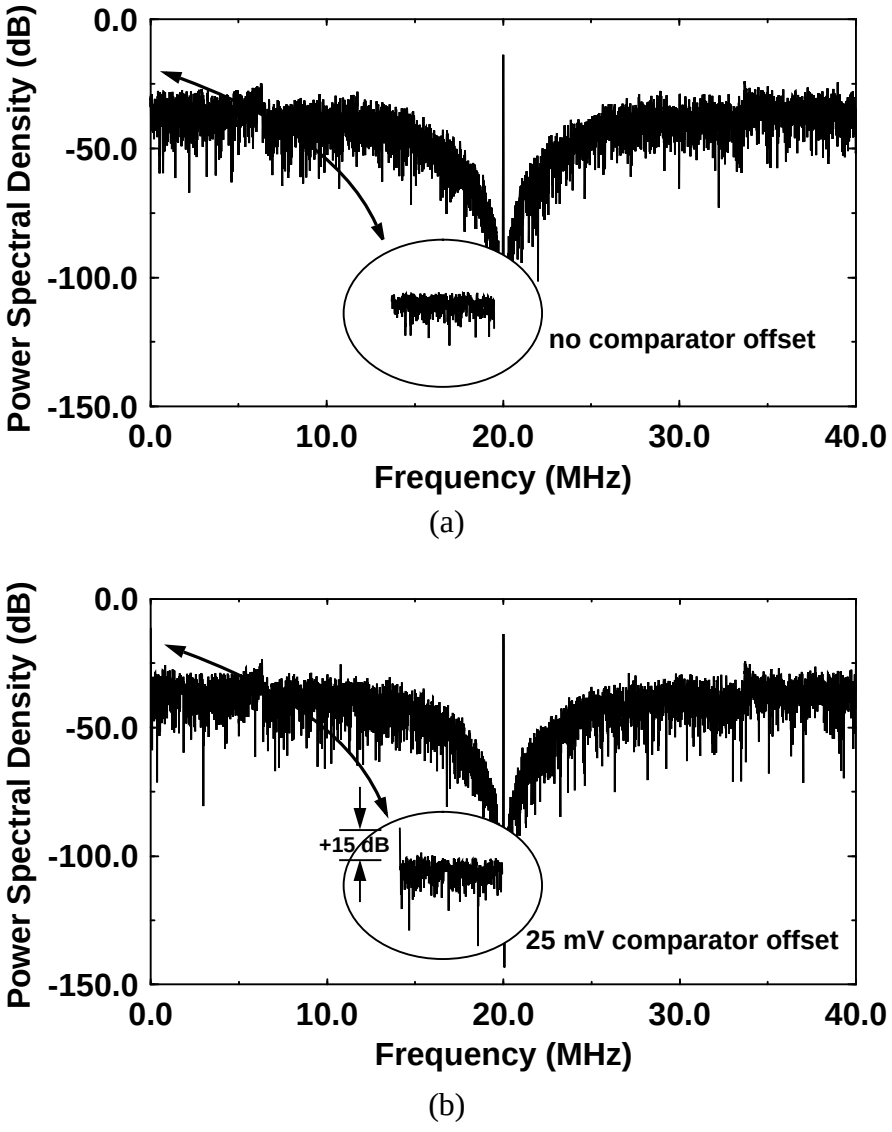


Figure 4.4: Output spectrum with a close-up view around dc when the comparator offset is (a) zero, and (b) $\Delta/40$, where $\Delta = 1$ V.

signal passband through modulator nonlinearities, as described in Section 3.3. An example of a high-level, spurious dc tone in the output spectrum is illustrated in Figure 4.4(b), which depicts the results of a behavioral simulation of the modulator in Figure 4.1 that is ideal except for a comparator offset of $\Delta/40$, where Δ is the step size of the two-level quantizer. If $\Delta = 1$ V, then a comparator offset of $\Delta/40$ is only 25 mV. Offsets of this mag-

nitude are not uncommon if the comparator is implemented using a simple regenerative latch, as is commonly done in single-bit, lowpass and bandpass modulators [14], [50], [56].

Insofar as noise tones are concerned, bandpass modulators can be more sensitive to offsets than their lowpass counterparts. Offsets in bandpass modulators are not necessarily suppressed by the noiseshaping properties of the system. For example, if comparator offset is modeled as a dc level added at the input to the comparator, it is easy to see that the offset is shaped by the same noise transfer function as the quantization noise. For the proposed $f_s/4$ modulator, the noise transfer function, $NTF(z) = (1 + z^{-2})^2$, has a maximum at dc and at $f_s/2$, indicating that the modulator does not suppress tones at these frequencies. In contrast, the noise transfer function of a lowpass modulator usually includes one or more zeros at dc, meaning that the same properties of a lowpass modulator that suppress quantization noise also suppress the effects of comparator offset.

4.1.5 Timing Jitter

As in any sampling system, clock jitter in bandpass sigma-delta modulators results in non-uniform sampling and can introduce errors into the sampled values. In bandpass modulators, the frequency of the input signal can be a substantial fraction of the sampling frequency. Therefore, the acceptable bound on clock jitter is tighter than for lowpass modulators, in which the input varies slowly with respect to the sampling clock. For example, in an $f_s/4$ modulator, the input signal can change by as much as one-half of the two-level quantizer step size, Δ, between samples. With such large slew rates, the input can no longer be considered quasi-static, as is often assumed in the lowpass case when the input signal is often only one- or two-hundredths of the sampling frequency. Intuitively, it can be seen that when the input is quasi-static with respect to the modulator sampling clock, small errors in the exact sampling times generally do not affect the final value because the input signal varies slowly between sampling instances. This is clearly not the case for an $f_s/4$ bandpass modulator. In the following assessment of jitter in the sampling clock, it is assumed that the bandpass modulator has been implemented using a conventional

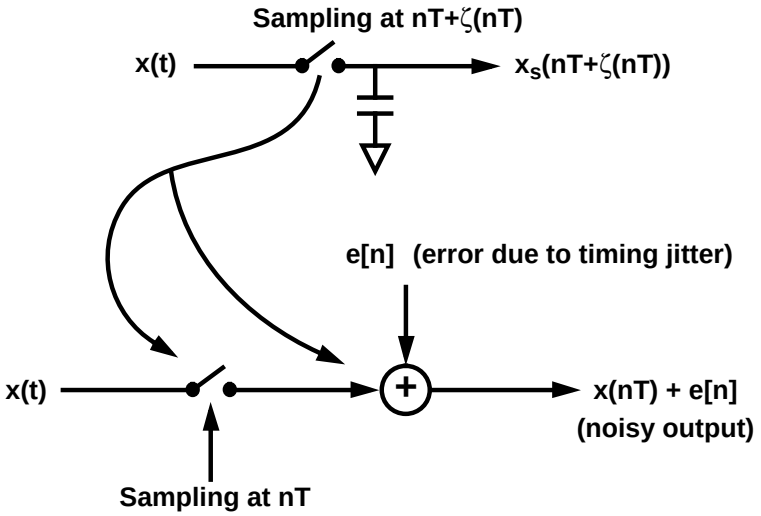


Figure 4.5: A discrete model of the sampling process when the sampling times, *nT*, are perturbed by a random process, $\zeta(t)$.

switched-capacitor circuit structure that is insensitive to jitter once the input signal has been sampled. Therefore, the degradation in the system performance attributed to jitter can be predicted solely by determining the effect of jitter on the sampling of the input signal.

The analysis of jitter begins with the sampling model shown in Figure 4.5. The input signal, $x(t)$, is assumed to be sampled at $t = nT + \zeta(nT)$, where $\zeta(t)$ is a random process that models the perturbation of the actual sampling instant from the ideal *nT*. The error that results from jittered sampling, $e[n]$, is defined as

$$e[n] = x(nT + \zeta(nT)) - x(nT) \ . \tag{4.3}$$

Because $\zeta(nT) << T$, (4.3) can be approximated using a first-order Taylor expansion as

$$\begin{aligned} e[n] &\approx x(nT) + \zeta(nT)\dot{x}(nT) - x(nT) \\ &= \zeta(nT)\dot{x}(nT) \end{aligned} \tag{4.4}$$

where $\dot{x}(nT)$ is the derivative of $x(t)$ at $t = nT$. Therefore, for a sinusoidal input, $x(t) = A\sin(2\pi f_x t)$, the error due to sampling that has been jittered by random process $\zeta(t)$ is [74]

$$e[n] = \zeta[n] A 2\pi f_x \cos(2\pi f_x nT) \; . \tag{4.5}$$

The autocorrelation of (4.5) is

$$\begin{aligned} R_e[m] &= E\{e[n]e[n+m]\} \\ &= \frac{A^2}{2}(2\pi f_x)^2 R_\zeta[m]\cos(2\pi f_x mT) \; . \end{aligned} \tag{4.6}$$

The power spectral density, $S_e(f)$, of $e[n]$ is obtained by taking the Fourier transform of (4.6) [75]. The following intermediate Fourier transforms are useful in arriving at the final expression [18]:

$$\frac{A^2}{2}(2\pi f_x)^2 R_\zeta[m] \;\leftrightarrow\; \frac{A^2}{2}(2\pi f_x)^2 S_\zeta(f) \tag{4.7}$$

and

$$\cos(2\pi f_x mT) \;\leftrightarrow\; \frac{1}{2T}\sum_{k=-\infty}^{\infty}[\delta(f - f_x + kf_s) + \delta(f + f_x + kf_s)] . \tag{4.8}$$

It is also necessary to use the modulation property of discrete-time Fourier transforms:

$$x[n]y[n] \;\leftrightarrow\; \frac{1}{f_s}\int_{-f_s/2}^{f_s/2} X(f - \hat{f})Y(\hat{f})d\hat{f} \; . \tag{4.9}$$

From (4.7), (4.8), and (4.9), it follows that the power spectral density, $S_e(f)$, is

$$\begin{aligned} S_e(f) = \frac{A^2}{4}(2\pi f_x)^2 \times \\ \int_{-f_s/2}^{f_s/2} S_\zeta(f - \hat{f})\left(\sum_{k=-\infty}^{\infty}[\delta(\hat{f} - f_x + kf_s) + \delta(\hat{f} + f_x + kf_s)]\right) d\hat{f} \quad , \end{aligned} \tag{4.10}$$

which, upon interchanging the integration and summation, is

$$S_e(f) = \frac{A^2}{4}(2\pi f_x)^2 \times \sum_{k=-\infty}^{\infty} \left\{ \int_{-f_s/2}^{f_s/2} S_\zeta(f-\hat{f})[\delta(\hat{f} - f_x + k f_s) + \delta(\hat{f} + f_x + k f_s)]\, d\hat{f} \right\} \quad . \tag{4.11}$$

Equation (4.11) can be simplified for two instructive cases. First, if the jitter, $\zeta(t)$, has a narrowband spectrum with a bandwidth much less than f_x, the power spectral density of the error reduces to

$$S_e(f) = \frac{A^2}{4} \times (2\pi f_x)^2 \times [S_\zeta(f - f_x) + S_\zeta(f + f_x)] \quad , \qquad -\frac{f_s}{2} < f < \frac{f_s}{2} \quad . \tag{4.12}$$

One example of a narrowband jitter process is when the sampling clock is derived from an oscillator with short-term instabilities that result in sideband skirts centered around the frequency of oscillation. In this case, (4.12) indicates that the phase noise skirts of the oscillator are scaled and replicated around the frequency of the input signal, f_x [74]. This situation is depicted for an $f_s/4$ modulator in Figure 4.6. As seen therein, upconverted $1/f$ and wideband noise results in narrowband skirts around the oscillator fundamental [76]. These phase noise skirts are then convolved with the signal tone near $f_s/4$. Clearly, the additional noise in the signal passband directly degrades the inband signal-to-noise ratio. Therefore, it is important to insure that the sampling clock is derived from an oscillator with good close-in phase noise performance. In Chapter 7, experimental results are presented that qualitatively confirm the degradation of the inband signal-to-noise ratio that occurs when the modulator is driven by a sampling clock with a high phase noise.

In a second case, if the jitter is a white noise process such that the errors in the sampling time are uncorrelated from one sampling instance to another, then the power spectral density of the discrete-time jitter process is

$$S_\zeta(f) = \frac{\sigma_\zeta^2}{f_s} \quad , \qquad -\frac{f_s}{2} < f < \frac{f_s}{2} \quad . \tag{4.13}$$

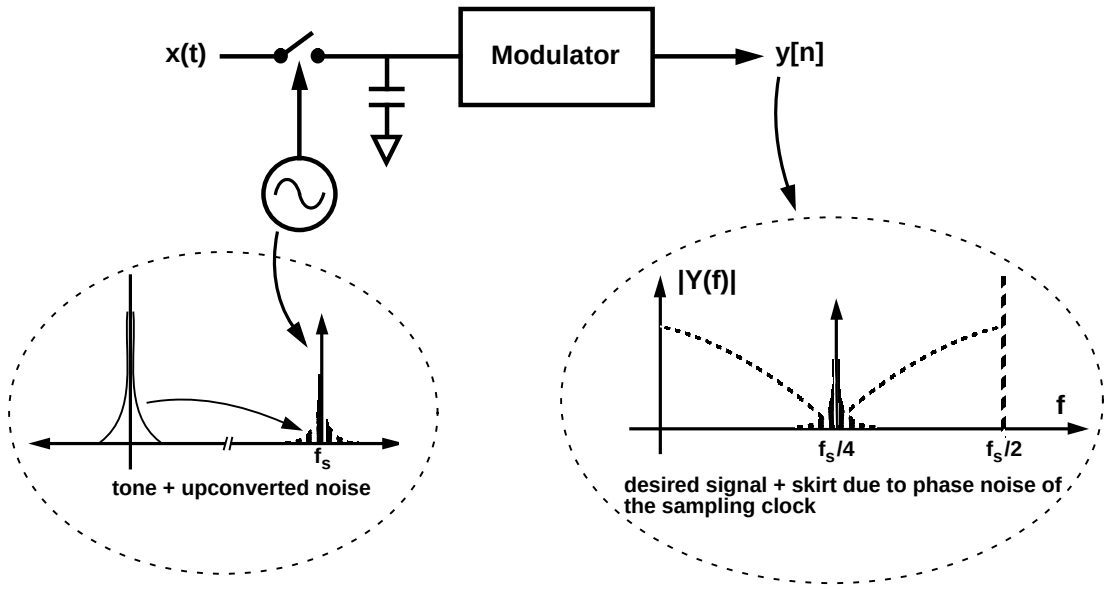


Figure 4.6: Degradation of the inband signal-to-noise ratio due to a sampling clock derived from an oscillator with high phase noise sidebands.

where σ_ζ^2 is the variance of the jitter. From (4.11) and (4.13), it follows that the total power of the jitter-induced error is [14]

$$P_e = \int_{-f_s/2}^{f_s/2} S_e(f)df = \frac{A^2}{4}(2\pi f_x)^2(2\sigma_\zeta^2) \tag{4.14}$$

$$= \frac{A^2}{2}(2\pi f_x)^2\sigma_\zeta^2 \quad .$$

Because the error caused by wideband jitter is evenly distributed throughout the sampling bandwidth, $-f_s/2$ to $f_s/2$, the power of the jitter-induced error in the signal passband is given by (4.14) divided by the oversampling ratio, M. Several trends can be predicted from (4.14). As the standard deviation of the jitter, σ_ζ, increases by 10×, the jitter-induced noise power increases by 20 dB. For a fixed σ_ζ, if the input amplitude increases by 2×, the jitter-induced noise power will increase by 6 dB. These trends are confirmed by a behav-

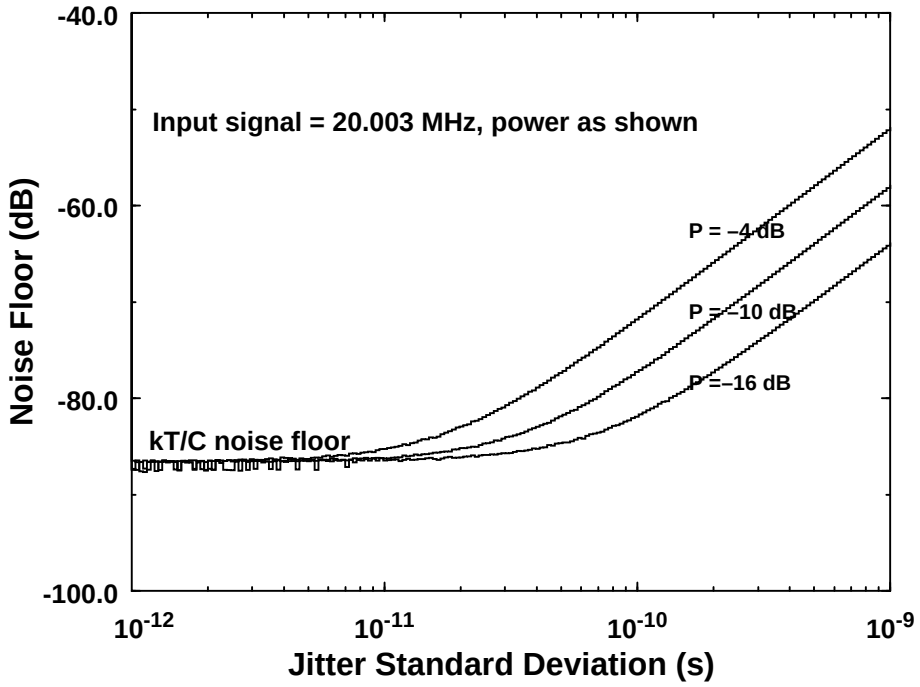


Figure 4.7: Behavioral simulation showing the broad increase in the noise floor that occurs as the standard deviation of the jitter increases.

ioral simulation of the modulator in Figure 4.1 in which jitter is modeled by adding a random error ζ, which has a zero mean and σ_ζ^2 variance, to the ideal sampling times, *nT*. Wideband noise is also added at the input to simulate the effect of *kT*/*C* noise. As indicated in Figure 4.7, when the jitter-induced noise begins to predominate over the *kT*/*C* noise floor, it is seen that the noise floor increases by 20 dB for every 10× increase in the standard deviation of the jitter. It is also observed that for a given jitter standard deviation, the noise floor increases by 6 dB as the amplitude of the input signal is doubled.

4.2 High Frequency Impairments

At high sampling speeds, the performance of the proposed fourth-order modulator depicted in Figure 4.1 is limited primarily by the nonideal behavior of the bandpass resonators. The ideal resonator has a biquadratic transfer function of

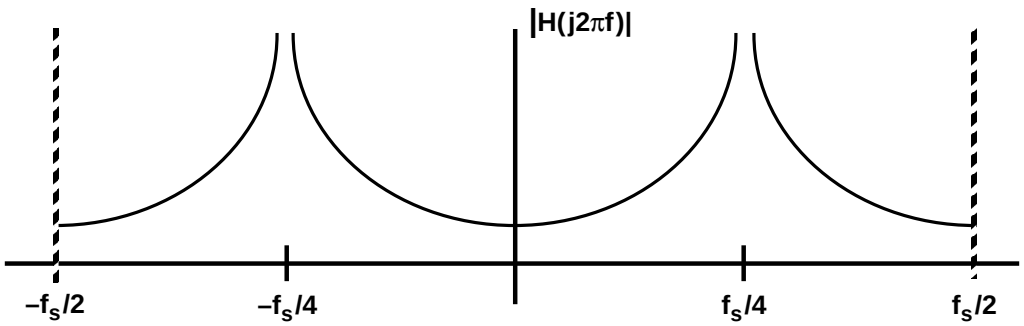


Figure 4.8: Ideal $f_s/4$ resonator magnitude response.

$$H(z) = G \cdot \frac{z^{-2}}{1 + z^{-2}} \tag{4.15}$$

where G is the gain of the resonator. As illustrated in Figure 4.8, the magnitude of (4.15) peaks at $f_s/4$.

Nonidealities in the operational amplifiers used to implement the resonator contribute potentially significant errors to (4.15). In the presence of finite dc gain and limited amplifier bandwidth, the resonator transfer function takes on the form

$$H(z) = G \cdot (1 - \varepsilon_a) \cdot \frac{z^{-2}}{1 + \varepsilon_b z^{-1} + (1 - \varepsilon_c) z^{-2}} \tag{4.16}$$

where ε_a, ε_b, and ε_c model small deviations from the ideal transfer function. The factors ε_a, ε_b, and ε_c limit the height of the peak in the magnitude response and shift the peak away from $f_s/4$.

The impact of limitations in the operational amplifier is especially severe if the biquadratic resonator transfer function is implemented using conventional switched-capacitor structures, such as the undamped, two-integrator loop illustrated in Figures 4.9(a) and (b) [67]. In this topology, the transfer function is synthesized with two operational amplifiers enclosed within a single feedback loop. As a consequence, each output sample of the resonator includes errors introduced by both amplifiers; the errors combine in an additive

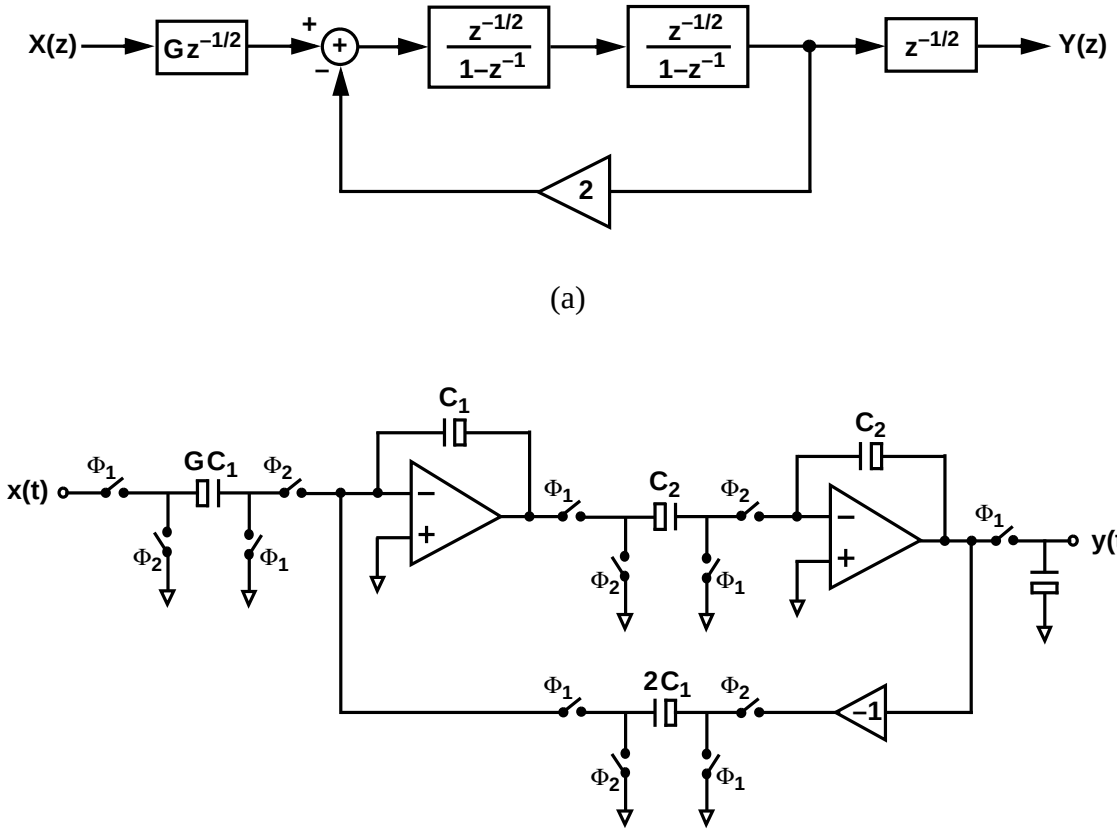


Figure 4.9: (a) Block and (b) circuit diagram of an $f_s/4$ resonator implemented using a two-integrator loop.

manner, and this accumulation of error can result in large deviations from the ideal response of (4.15). In particular, as the sampling rate of the two-integrator loop resonator increases, the error terms, ε_a, ε_b, and ε_c, grow in magnitude, compromising the ability of a modulator implemented using such resonators to attenuate the inband noise centered at $f_s/4$.

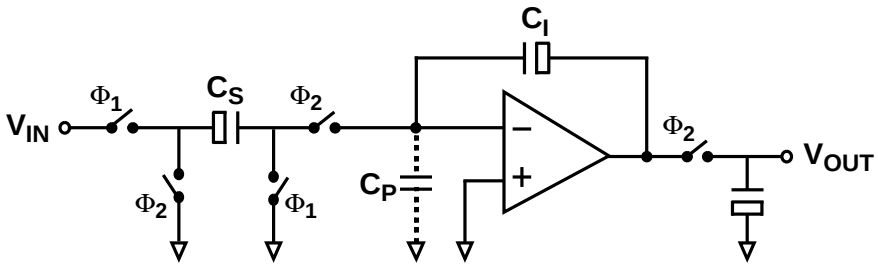


Figure 4.10: Switched-capacitor integrator with the output delayed by one-half sample period.

4.2.1 Analysis of the Two-Integrator Loop

The effect of nonideal operational amplifiers on the behavior of switched-capacitor circuits has been analyzed extensively [77], [78], and these analyses can be applied toward understanding the behavior of two-integrator loop resonators at high sampling rates. Because a switched-capacitor integrator of the type depicted in Figure 4.10 is the key constituent of a two-integrator loop resonator, degradation in the performance of such a resonator can be studied by considering how nonidealities in the integrators introduce errors into its transfer function, (4.15). In the analysis that follows, it is demonstrated that incomplete amplifier settling can limit the performance of a two-integrator loop resonator to a greater extent than either finite dc gain or random timing jitter. For simplicity, the errors contributed by finite operational amplifier gain are considered separately from those errors arising from limited amplifier bandwidth.

4.2.1.1 Errors Owing to Finite DC Operational Amplifier Gain

In the presence of finite operational amplifier gain, A, the switched-capacitor integrator implementation in Figure 4.10 has the transfer function

$$H(z) = \frac{C_S}{C_I} \cdot (1 - \delta_1) \cdot \frac{z^{-1/2}}{1 - (1 - \gamma_1)z^{-1}} \tag{4.17}$$

where the terms δ_1 and γ_1 model perturbations in the gain and pole locations of the integrator, respectively, and are given by

$$\delta_1 = \frac{1}{A}\left(1 + \frac{C_S}{C_I}\right) \tag{4.18}$$

and

$$\gamma_1 = \frac{\frac{1}{A}\left(\frac{C_S}{C_I}\right)}{1 + \frac{1}{A}\left(1 + \frac{C_S}{C_I}\right)} \quad . \tag{4.19}$$

The effect of finite amplifier gain on the resonator of Figure 4.9(b) is assessed by modeling the two, nominally identical, switched-capacitor integrators with (4.17) and independent error terms, δ_1, γ_1, δ_2, and γ_2. The system gains of both integrators, C_S/C_I, are chosen to be one. With this representation, the nonideal transfer function of the resonator is approximated by

$$H(z) = (1 - \delta_1 - \delta_2) \cdot \frac{z^{-2}}{1 + (\gamma_1 + \gamma_2 - 2\delta_1 - 2\delta_2)z^{-1} + (1 - \gamma_1 - \gamma_2)z^{-2}} \tag{4.20}$$

when second-order terms are neglected since they are much less than one. Errors δ_1, γ_1, δ_2, and γ_2 have the effect of causing the poles of $H(z)$ to shift away from $\pm f_s/4$, and off of the unit circle ($|z| = 1$). The new pole locations are

$$p_1, p_2 = \frac{2\delta_1 + 2\delta_2 - \gamma_1 - \gamma_2 \pm \sqrt{(\gamma_1 + \gamma_2 - 2\delta_1 - 2\delta_2)^2 - 4(1 - \gamma_1 - \gamma_2)}}{2(1 - \gamma_1 - \gamma_2)} \quad . \tag{4.21}$$

For small perturbations, namely δ_1, γ_1, δ_2, and $\gamma_2 << 1$, the pole locations, (4.21), simplify to

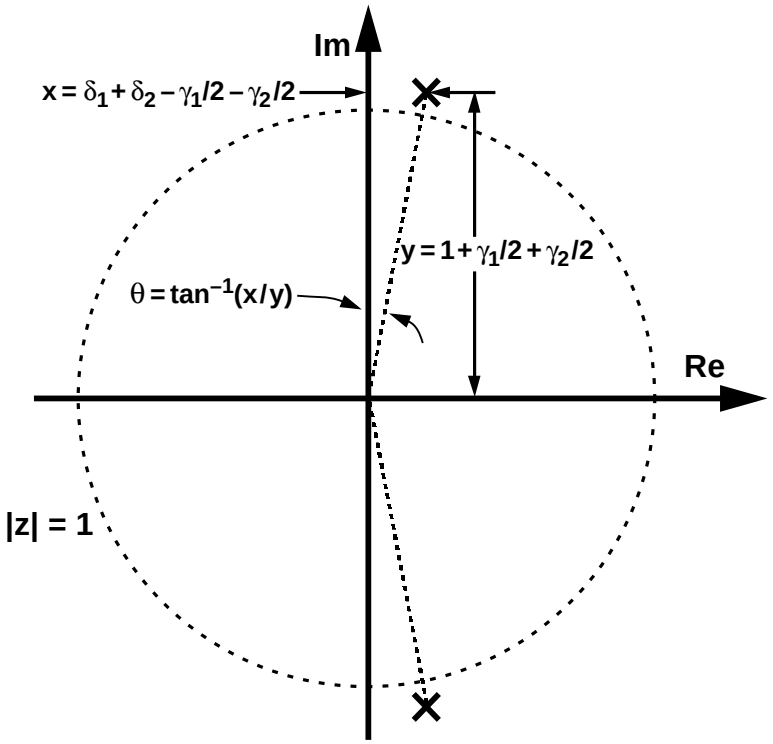


Figure 4.11: Pole locations of the $f_s/4$ resonator transfer function under the influence of finite dc operational amplifier gain.

$$p_1, p_2 \approx \frac{(2\delta_1 + 2\delta_2 - \gamma_1 - \gamma_2)}{2} \pm j\left(1 + \frac{\gamma_1}{2} + \frac{\gamma_2}{2}\right). \tag{4.22}$$

A geometric representation of (4.22) is illustrated in Figure 4.11. The deviation, θ, of the resonator center frequency from $\pi/2$ is

$$\theta = \arctan \frac{\dfrac{(2\delta_1 + 2\delta_2 - \gamma_1 - \gamma_2)}{2}}{1 + \dfrac{\gamma_1}{2} + \dfrac{\gamma_2}{2}}, \tag{4.23}$$

which for small δ_1, δ_2, γ_1, and γ_2, is

$$\theta \approx \delta_1 + \delta_2 - \frac{\gamma_1}{2} - \frac{\gamma_2}{2} \quad . \tag{4.24}$$

Thus, for small perturbations δ_1, γ_1, δ_2, and γ_2, the error in the resonator center frequency, f_o, is

$$\Delta f_o \approx -\theta \times \frac{f_s}{2\pi} = -\theta \times \frac{4 f_o}{2\pi} = \left(\frac{\gamma_1}{2} + \frac{\gamma_2}{2} - \delta_1 - \delta_2\right) \times \frac{2 f_o}{\pi} \quad , \tag{4.25}$$

so the fractional deviation in the resonator center frequency is

$$\frac{\Delta f_o}{f_o} \approx \frac{\gamma_1 + \gamma_2 - 2\delta_1 - 2\delta_2}{\pi} \quad . \tag{4.26}$$

If the switched-capacitor integrators in Figure 4.9(b) are implemented with operational amplifiers having a nominal dc gain of 60 dB, it follows from (4.20) and (4.26) that the magnitude peak of the resonator transfer function shifts by only 0.2% of f_o, or 40 kHz, when its ideal center frequency is 20 MHz. Because of a fortuitous partial cancellation in (4.26) between perturbation terms γ_1, γ_2 and δ_1, δ_2, the deviation in f_o is relatively small, even with a modest amplifier gain of only 60 dB. Within the context of a bandpass modulator, this shift in the peak of the magnitude response of the resonator results in a corresponding shift in the minimum of the noise transfer function away from $f_s/4$.

The increase in inband noise in the fourth-order modulator of Figure 4.1 that results from finite amplifier gain has been estimated by means of behavioral simulations that model the constituent resonators with (4.20). Resonator perturbation terms, δ_1, γ_1 and δ_2, γ_2, were determined by assuming an amplifier gain of 60 dB. In a 200-kHz passband centered at $f_s/4$, the simulations show that the loss in dynamic range is approximately 5 dB in a modulator with performance that is limited solely by quantization noise.

In practice, the dynamic range of a modulator is often limited by circuit, rather than quantization noise. In such cases, the noise floor within the signal passband is determined by noise introduced at the input to the modulator, since this noise is not attenuated by noiseshaping. Sources of this unshaped noise include thermal noise in the first resonator,

as well as *kT/C* noise from the input sampling network. When the shaped quantization noise lies well below the noise floor within the passband, small shifts in the exact minimum of the noise transfer function have a negligible influence on the total inband noise. This is not true, however, if the fractional shift in f_o becomes large enough to begin shifting the large out-of-band quantization noise into the signal passband.

The above analysis is limited by the assumption that the response of the amplifier is linear across its entire output range. Under this assumption, a dc gain of only 60 dB is sufficient to avoid any appreciable loss in the dynamic range. In practice, however, higher dc gains may be needed to suppress harmonic distortion in the integrators that can result from nonlinearity in the amplifier transfer characteristic.

4.2.1.2 Errors Owing to Finite Operational Amplifier Bandwidth

In the presence of limited operational amplifier bandwidth, the switched-capacitor integrator of Figure 4.10 suffers from incomplete settling. If the integrator is assumed to settle linearly with a single-pole response, incomplete settling only manifests itself as an integrator gain error [14]. In this case, the transfer function of the integrator is

$$H(z) = \frac{C_S}{C_I} \cdot (1 - \varepsilon_1) \cdot \frac{z^{-1/2}}{1 - z^{-1}} \tag{4.27}$$

where gain error term, ε_1, is

$$\varepsilon_1 = e^{-T/\tau} \ . \tag{4.28}$$

T is the time allotted for settling, and τ is the closed-loop time constant of the integrator. If the resonator is implemented using two-phase, non-overlapping clocks with 50% duty cycles, the allowable settling time, T, is slightly less than $T_s/2$, where $1/T_s = f_s$, the sampling frequency. The closed-loop time constant of the integrator, τ, is approximately

$$\tau \approx \frac{1}{2\pi f_u} \cdot \frac{C_S + C_I + C_P}{C_I} \tag{4.29}$$

where f_u is the unity-gain frequency of the operational amplifier and C_P is the parasitic capacitance at the input to the operational amplifier. As the sampling rate is increased, the available settling time, *T*, decreases, and the gain error in (4.27) becomes increasingly large.

As a caveat, it should be noted that, in practice, settling in switched-capacitor circuits is rarely governed by a strictly linear, single-pole response. Rather, the settling process usually includes a signal-dependent slewing component and is influenced by nondominant poles of the amplifier [49], [79], as well as finite switch resistances in the switched-capacitor network. In such cases, errors in a switched-capacitor integrator due to incomplete settling are understated by (4.27) and (4.28), with nonlinearities in the settling process not even reflected in these expressions. For tractability, only linear settling is considered in this analysis.

The effect of incomplete, but linear, integrator settling upon the resonator in Figure 4.9(b) can be assessed by modeling the two switched-capacitor integrators with (4.27) and independent gain error parameters ε_1 and ε_2. When second-order terms are neglected, the perturbed resonator transfer function is found to be

$$H(z) = (1-\varepsilon_1-\varepsilon_2)\cdot\frac{z^{-2}}{1-(2\varepsilon_1+2\varepsilon_2)z^{-1}+z^{-2}} \quad . \tag{4.30}$$

From (4.30) and the analysis in the previous section for finite dc gain, it follows that the fractional shift in resonator center frequency, f_o, due to incomplete settling is approximately

$$\frac{\Delta f_o}{f_o} \approx -\frac{2\varepsilon_1+2\varepsilon_2}{\pi} \quad . \tag{4.31}$$

The unfortunate implication of (4.28), (4.30), and (4.31) is that as the sampling frequency is increased, thus decreasing the time allotted for settling, *T*, the fractional shift in f_o becomes larger, and the minimum of the modulator noise transfer function deviates by an

increasing amount from $f_s/4$. Eventually, the noise minimum moves out of the signal passband all together.

As an example, if the modulator shown in Figure 4.1 operates at a sampling rate of 80 MHz, from two-phase, non-overlapping clocks, less than 6 ns during each clock phase is available for settling. If it is further assumed that a high bandwidth amplifier design results in a closed-loop time constant, τ, of approximately 1.3 ns, the settling time is limited to roughly 4τ. From (4.30) and (4.31), it then follows that the center frequency of the resonators will shift by -470 kHz. Under these assumptions, the penalty in dynamic range can be assessed with MIDAS by modeling the constituent resonators using (4.30). Simulations show that the dynamic range in a 200 kHz passband centered at $f_s/4$ is reduced by 30 dB if the modulator is limited by quantization noise.

As discussed in the previous subsection, the loss in dynamic range due to resonator degradation will be less severe if a modulator is limited by thermal, rather than quantization, noise. However, as is evident from (4.28) and (4.31), the shift in the minimum of the noise transfer function from $f_s/4$ increases with increasing sampling rate, in contrast to the shift that results from finite amplifier gain. Consequently, at the high sampling rates needed to digitize signals at conventional radio IFs, the minimum of the noise transfer function may shift by an amount large enough to move high levels of nominally out-of-band quantization noise into the passband.

4.3 Summary

The design of a fourth-order, $f_s/4$ modulator has been considered at the system level. Modifications to the canonical $f_s/4$ topology were proposed in order to address potential limitations inherent in the architecture. Namely, a delay has been included in the forward path of both resonators to improve the settling performance in a switched-capacitor implementation of the modulator. Also, the system gains of the resonators have been scaled to constrain the signal swings at internal modulator nodes.

Important system-level nonidealities were analyzed in order to assess their impact on the performance of the proposed $f_s/4$ modulator. It was shown that electronic noise and timing jitter effectively raise the level of noise in the signal passband. If the noise is distributed equally over the sampling bandwidth, $-f_s/2$ to $f_s/2$, then the modulator attenuates the amount of noise in the passband through oversampling or a combination of both oversampling and noiseshaping. However, in cases where the injected noise is concentrated within the signal band, there may be a more severe loss in the inband signal-to-noise ratio. This is the situation when the sampling clock is derived from an oscillator with a poor close-in phase noise specification. In this case, the sideband skirts of the oscillator fundamental are scaled and replicated around the input signal. It was also demonstrated that a modest amount of comparator offset could result in out-of-band tones that are 15 dB above the noise floor near dc or $f_s/2$. These tones are troublesome because they can limit the dynamic range of the modulator and can mix with the input signal through nonlinearities and fall into the passband.

In a switched-capacitor implementation, the effects of finite dc gain and limited settling time in the operational amplifier were shown to directly degrade the transfer functions of the resonators that constitute the modulator. As the sampling frequency is increased, the error introduced by finite settling can cause the center frequency of the resonators to shift by several hundred kHz away from the center of the signal passband, thus moving nominally out-of-band quantization noise into the passband. This degradation becomes acute at the sampling frequencies necessary to digitize signals centered at frequencies above 10 MHz. Fortunately, it is possible to attack this limitation through the use of *N*-path filter topologies. As discussed in Section 4.1, $f_s/4$ modulators derived via the dc-to-$f_s/4$ transformation, (3.23), including the proposed topology depicted in Figure 4.1, can be easily partitioned into two independent time-interleaved paths that permit a doubling of the allowable circuit settling time for a given sampling frequency. In the following chapter, a review of *N*-path filter theory is presented, followed by a description of the chosen two-path implementation of the proposed $f_s/4$ modulator.

Chapter 5

N-Path Design Issues

The previous chapter proposed a system-level design for a fourth-order, $f_s/4$ modulator based upon the dc-to-$f_s/4$ transformation, (3.23). It was also observed that a key motivation for choosing an architecture based on this transformation is that the resulting modulator is especially suited for implementation using two-path circuits. The use of a two-path topology allows the circuit blocks in the critical path of the modulator to operate at a 2× slower sampling rate than the overall throughput of the modulator, which implies a doubling of the allowable circuit settling time.

This chapter begins by introducing the general concept and motivation for *N*-path filtering. The essential input-output relationships for *N*-path systems are stated, with detailed derivations given in Appendix B. It is shown that by applying *N*-path principles, the resonators of the proposed fourth-order, $f_s/4$ modulator can be implemented easily by interleaving two highpass filters. This results in a simple resonator topology that resists errors due to circuit nonidealities at high sampling speeds. However, this new topology is still susceptible to errors arising from noise feedthrough, as well as the additional problem of path mismatch. The impact of these nonidealities is analyzed. Finally, a complete block diagram of the proposed two-path modulator implementation is shown, and its operation is discussed.

5.1 *N*-Path Filter Theory

The design of a filter that must operate at high sampling rates and/or synthesize a very selective passband may sometimes be simplified by partitioning the filter into *N* independent paths, and clocking these paths with an *N*-phase, non-overlapping clock [80]-[85].

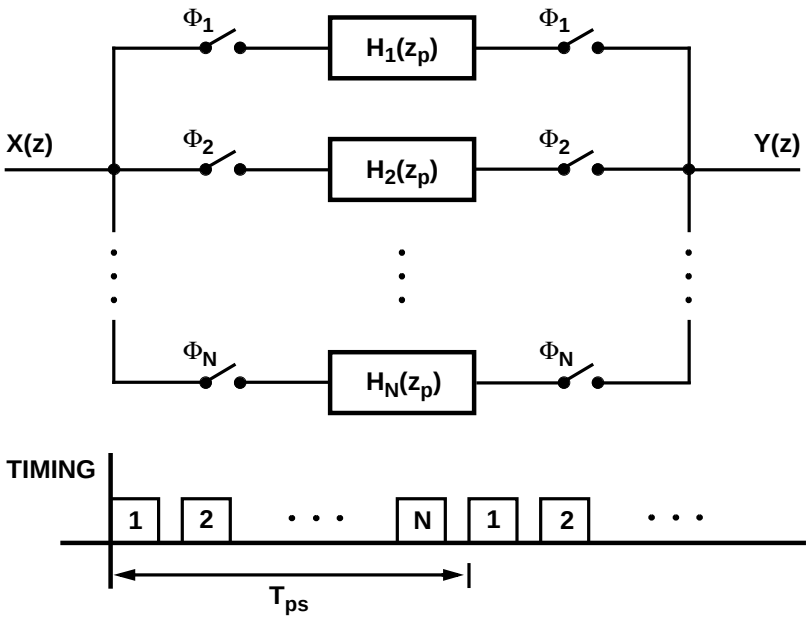


Figure 5.1: Generalized *N*-path filter structure.

The generalized *N*-path filter topology is illustrated in Figure 5.1. The *N* filters comprising the structure, $H_1(z_p)$, $H_2(z_p)$, … ,$H_N(z_p)$, are nominally identical. From the timing diagram in Figure 5.1, it is seen that the paths are clocked in an interleaved fashion. Thus, the sampling rate of each path filter is reduced by a factor of *N* relative to the effective throughput rate of the overall *N*-path structure.

If the paths in the *N*-path filter of Figure 5.1 are assumed to match perfectly, such that $H_1(z_p) = H_2(z_p) = \ldots = H_N(z_p) = H(z_p)$, then the *z*-domain transfer function of the structure is

$$H_T(z) = \frac{Y(z)}{X(z)} = H(z_p)\Big|_{z_p = z^N} \tag{5.1}$$

where $H(z_p)$ denotes the transfer function of each identical path filter [85]. In this expression, z_p corresponds to the z variable of a single path, and z_p^{-1} is interpreted as a single delay with respect to the sampling rate of a single path. z^{-1} represents a single delay

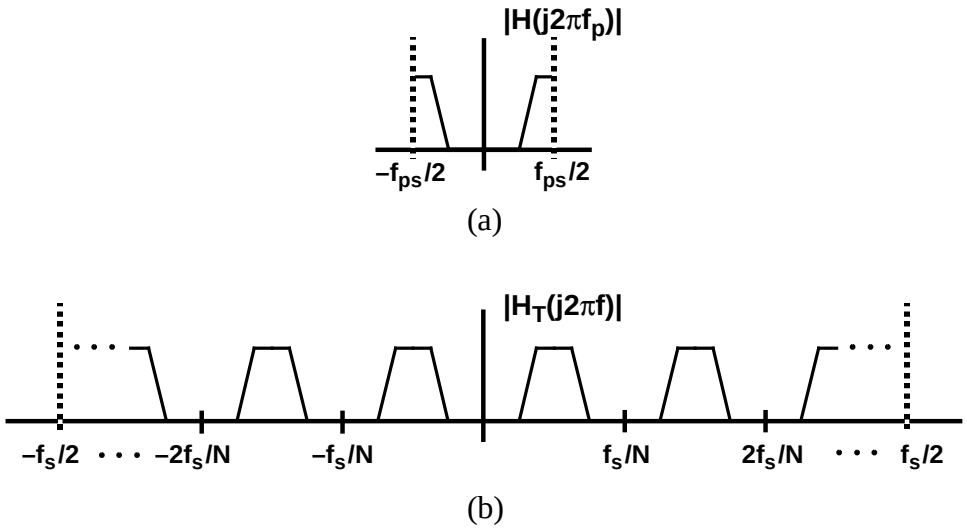


Figure 5.2: Nyquist-band frequency response of (a) an individual path, and (b) an *N*-path filter.

with respect to the effective throughput rate of the *N*-path filter, as implied by the relationship $z_p = z^N$. A detailed derivation of (5.1) can be found in Appendix A.

The frequency response of the *N*-path filter shown in Figure 5.1 is found by substituting $z = e^{j2\pi f T_s}$ into (5.1), which yields the expression

$$H_T(e^{j2\pi f T_s}) = H(e^{j2\pi f T_s N}). \tag{5.2}$$

Interestingly, this expression indicates that the frequency response of the overall *N*-path system is identical to that of a single path, except that in the *N*-path system, the Nyquist frequency is *N* times larger. This point is seen more clearly by considering the graphical example depicted in Figure 5.2. Consider a path filter with a certain highpass transfer characteristic, such as that shown in Figure 5.2(a). The frequency response of this path is periodic with respect to the path sampling frequency, f_{ps}, and the Nyquist frequency of this path is $f_{ps}/2$. In Figure 5.2(b) it is seen that the frequency response of the overall *N*-path system is exactly equal to that of the individual path, except that the Nyquist frequency of the *N*-path filter is $f_s/2$, which exceeds that of an individual path by a factor of *N*. As a

result, the *N*-path filter can process signals that fall beyond the Nyquist limitation of each individual path filter without introducing any distortion due to aliasing, despite the apparent contradiction that the input signal is potentially subsampled by every path.

Insofar as subsampling is concerned, each path filter does sample the input signal, $x(t)$, at frequency f_{ps}, and therefore replicates the spectral content of $x(t)$ at multiples of f_{ps} in every path. However, the sampling clocks in subsequent paths are offset by increasing multiples of T_{ps}/N, as depicted in the timing diagram of Figure 5.1. Therefore, the phase of each path's aliases differs by multiples of $2\pi/N$ with respect to their counterparts in the other paths. The mathematical derivation of (5.1) presented in Appendix B shows that the phases of these aliases are spaced such that when the path outputs are interleaved, the $N-1$ aliases not centered at baseband destructively cancel. If the matching between paths is perfect, no residual images remain in the output signal, $y(t)$, and the effective Nyquist frequency for the *N*-path filter is equal to $Nf_{ps}/2$, or $f_s/2$.

A consideration of Figure 5.2(b) also reveals that a highly selective bandpass response can be synthesized by interleaving path filters with sharp lowpass or highpass transfer functions. In this manner, the passband of a bandpass filter can be made much narrower relative to the filter sampling frequency than if the filter were to be implemented with a cascade of biquadratic sections that are clocked at the full output rate. In this work, this property is exploited to synthesize the desired $f_s/4$ resonator by interleaving two independent highpass path filters. Because a highpass building block is less complex than a biquadratic circuit of the type described in Chapter 4, a resonator based on these simpler highpass filters is likely to be less susceptible to the amplifier gain and settling errors analyzed for a biquadratic-based resonator.

5.2 Two-Path Resonator Design

The desired resonator transfer function, $H(z) = Gz^{-2} / (1 + z^{-2})$, can be expressed as a function of z_p in the following manner,

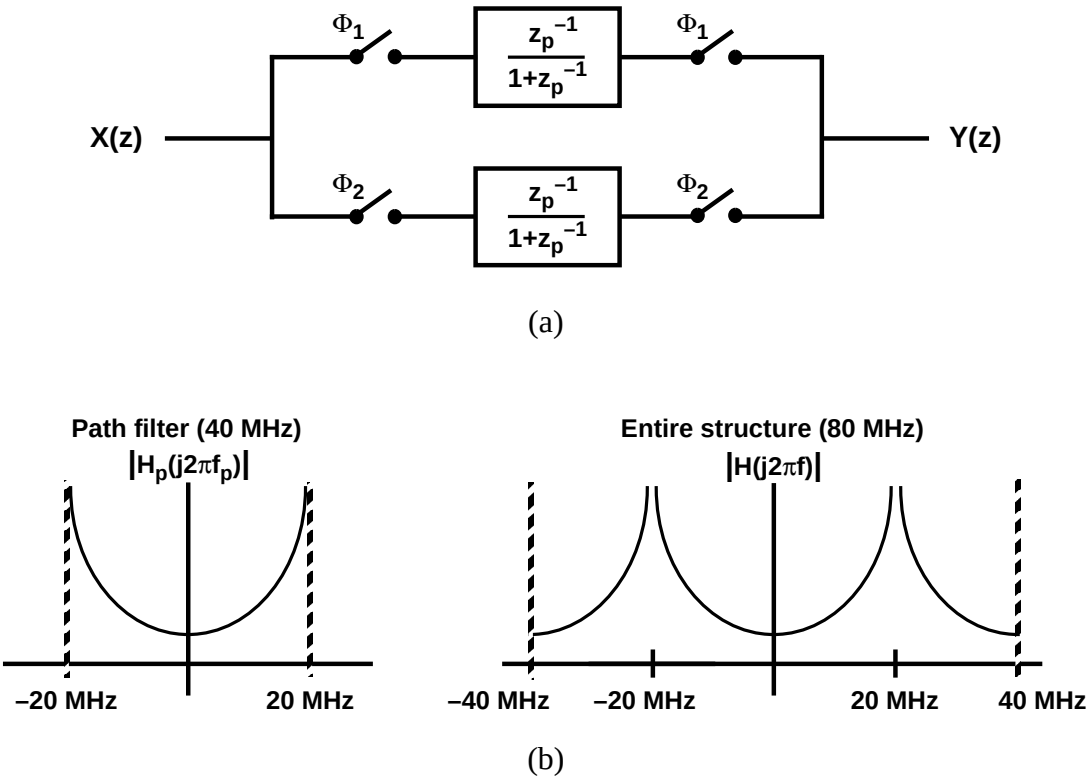


Figure 5.3: (a) Two-path implementation of an $f_s/4$ resonator, and (b) the frequency response of the path filter compared with that of the resonator.

$$H(z) = G \cdot \frac{z^{-2}}{1+z^{-2}} = G \cdot \left. \frac{z_p^{-1}}{1+z_p^{-1}} \right|_{z_p = z^2} . \tag{5.3}$$

Therefore, the $f_s/4$ bandpass resonator can be naturally partitioned into a two-path structure consisting of two nominally identical highpass filters, as illustrated in Figure 5.3(a). In Figure 5.3(b) the Nyquist-band frequency response of the path filters is compared with the response of the interleaved structure. The desired resonant peak at $f_s/4$ is implemented using highpass path filters that are clocked at one-half of the overall resonator output rate, so the demand on the amplifier settling is relaxed by a factor of two. It is also important to note that the highpass transfer function,

$$H(z_p) = G \cdot \frac{z_p^{-1}}{1 + z_p^{-1}} \tag{5.4}$$

can be implemented as a switched-capacitor filter with only one operational amplifier, as will be shown in the next chapter. Moreover, there is no interaction between this amplifier and its counterpart in the other path. Consequently, each resonator output sample will include errors due to finite dc gain and incomplete settling from only one amplifier, rather than two. The exact nature of the errors arising from amplifier limitations depends upon the particular switched-capacitor topology chosen to implement the highpass transfer function of (5.1) and is discussed in the Chapter 6, where the prototype implementation is described.

5.2.1 Noise Feedthrough

In the two-path resonator of Figure 5.3(a), fixed-pattern noise arising from clock feedthrough, offset, and other signal-independent errors manifests itself as tones at dc and at multiples of the path sampling frequency, $f_s/2$, where f_s is the sampling frequency of the modulator [85]. However, because the magnitude peak of the resonator is centered at $f_s/4$, these tones can largely be ignored because they lie far removed from the frequency band of interest at $f_s/4$. In the experimental modulator, since the sampling frequency is 80 MHz signal-independent errors and offsets introduce tones into the output spectrum at dc, ±40 MHz, ±80 MHz, etc. Because these tones lie well outside of the signal passband centered at $f_s/4$, they are rejected by the decimation filter that follows the modulator.

5.2.2 Transfer Function Mismatch

Gain and phase mismatch between the signal transfer functions in the two paths of presents a more serious problem than fixed-pattern noise because such mismatch compromises the suppression of mirror images of the desired signal that appear in the passband [85]. General expressions describing incomplete mirror-image suppression have been derived for the related case of asymmetry between A/D converters employed in a

time-interleaved array of converters [86]-[88]. A similar analysis can be applied to the two-path resonator. If the transfer functions of the two paths in Figure 5.3(a) are denoted by $H_1(z_p)$ and $H_2(z_p)$, where $z_p = z^2$ for this two-path structure, the output of the resonator can be expressed in the z-domain as

$$Y(z) = \frac{1}{2}(H_1(z^2) + H_2(z^2)) \cdot X(z) + \frac{1}{2}(H_1(z^2) - H_2(z^2)) \cdot X(-z) \ . \tag{5.5}$$

If $z = e^{j2\pi f T_s}$ is substituted into (5.5), the spectrum of *Y(z)* is found to be

$$\begin{aligned} Y\left(e^{j2\pi f T_s}\right) = \ & \frac{1}{2}\left(H_1\left(e^{j2\pi f 2T_s}\right) + H_2\left(e^{j2\pi f 2T_s}\right)\right) \cdot X\left(e^{j2\pi f T_s}\right) + \\ & \frac{1}{2}\left(H_1\left(e^{j2\pi f 2T_s}\right) - H_2\left(e^{j2\pi f 2T_s}\right)\right) \cdot X\left(e^{j2\pi (f - f_s/2)T_s}\right) \ . \end{aligned} \tag{5.6}$$

This equation indicates that the resonator output consists of a desired response that is the average of H_1 and H_2, together with a spurious mirror-signal response that depends entirely upon the difference between H_1 and H_2. If the gains of H_1 and H_2 are mismatched by 1%, (5.6) predicts that the undesired mirror signal in the output of the resonator will be suppressed by approximately 40 dB.

Because of gain and phase mismatch inherent in both resonators, the output of a modulator implemented using two-path resonators will contain an undesired image of the input signal at a mirror location centered around $f_s/4$, as illustrated in Figure 5.4. This image lies within the signal passband so it cannot be suppressed by filtering. Furthermore, for a given level of matching within the modulator, the degree of mirror signal suppression is likely to be worse than that predicted by (5.6) because both resonators undermine the suppression. Also, (5.6) does not account for other factors that limit the mirror signal suppression, such as systematic errors in the path sampling times and mismatched transistor switch networks in the path filters. Fortunately, because the mirror image is merely a scaled version of the desired signal, as opposed to being an unrelated and possibly much larger signal, only 25 dB of image suppression is considered adequate for many applications [89].

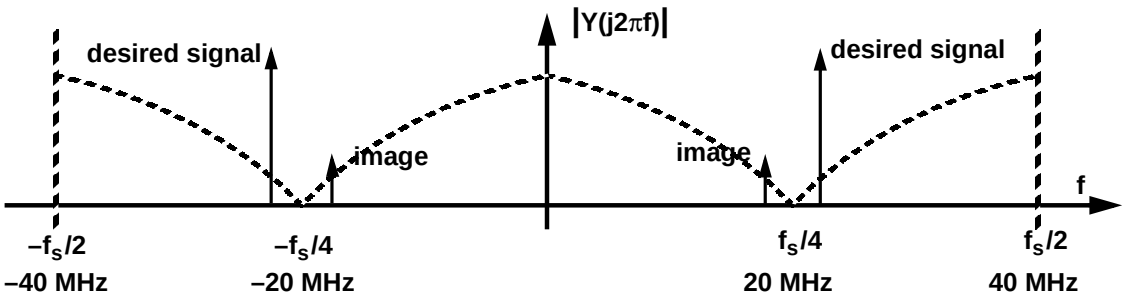


Figure 5.4: Mirror image of the signal introduced by gain and phase mismatches into the output spectrum of the modulator.

The incomplete mirror-signal suppression caused by path mismatch is analogous to the unwanted image that is introduced by phase and gain errors during conventional analog *I* and *Q* demodulation [90]. As it was shown in Chapter 2, if the *LO* signals are balanced in amplitude but differ in phase by 90 + ϕ degrees, the rejection of the undesired mirror signal is given by

$$IR = \left(\frac{\pi}{180} \cdot \frac{\phi}{2}\right)^2 \quad . \tag{5.7}$$

Without special trimming or analog tuning techniques, it is difficult to reduce the phase error between the *LO* signals significantly below 1° [91]. Therefore, assuming a phase error of 1°, the unwanted mirror signal will be suppressed by approximately 40 dB, which is comparable to what can be achieved by relying on path matching in the proposed two-path approach.

5.2.3 Timing Errors

Two types of timing errors, random and systematic, can affect the performance of the two-path resonator. If there is random jitter in the sampling clocks for the individual paths, Φ_1 and Φ_2, then the inband noise floor is degraded as analyzed in Section 4.1.5. However, if clock skew causes a systematic error in the sampling times, then the mirror image sup-

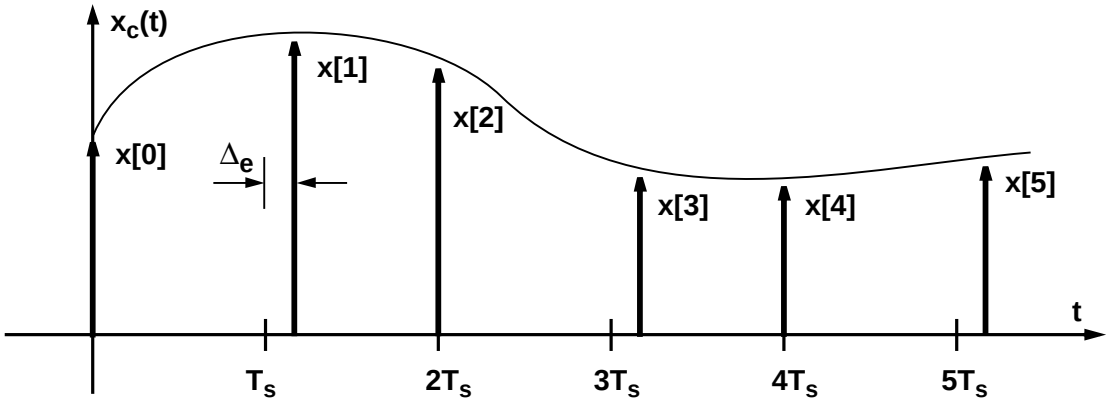


Figure 5.5: An example of a systematic timing error, Δ_e, that results when sampling a continuous-time signal, $x_c(t)$, with skewed two-phase clocks.

pression in the output of the resonator is compromised in a manner similar to when the path filter transfer functions are mismatched [92]. This effect is analyzed by examining the spectrum of a signal that has been sampled with a systematic timing error at every other sampling instance.

A systematic timing error between Φ_1 and Φ_2, Δ_e, is illustrated in Figure 5.5. It is seen that the continuous-time input signal, $x_c(t)$, is effectively sampled at $t = 0$, $T_s+\Delta_e$, $2T_s$, $3T_s+\Delta_e$, $4T_s$, $5T_s+\Delta_e$, … . If the discrete-time sequence, $x[n]$, is defined such that $x[0] = x(0)$, $x[1] = x(T_s+\Delta_e)$, $x[2] = x(2T_s)$, … , then it can be shown that the spectrum of $x[n]$ is [86]

$$X(e^{j2\pi f T_s}) = \frac{f_s}{2} \sum_{n=-\infty}^{\infty} X_c\left(f - n\frac{f_s}{2}\right)[1 + (-1)^n e^{j2\pi f \Delta_e} e^{-j\pi n \Delta_e f_s}] \ . \qquad (5.8)$$

In this expression, f_s refers to the overall sampling frequency of the two-path system, and $X_c(f)$ is the continuous-time Fourier transform of $x_c(t)$. For the case when $\Delta_e = 0$, (5.8) reduces to the familiar expression for the spectrum of a sampled signal

$$X(e^{j2\pi f T_s}) = f_s \sum_{n=-\infty}^{\infty} X_c(f - nf_s) \ . \tag{5.9}$$

Since (5.8) is the spectrum of a sampled signal, it is periodic with respect to f_s. Therefore, assuming that $x_c(t)$ is bandlimited to $f_s/2$, the spectral content between $-f_s/2$ and $f_s/2$ is completely defined by the $n = 0$, 1, and –1 terms in (5.8). The desired signal is the $n = 0$ term, which is

$$X_{sig}(f) = f_s X_c(f) \ , \tag{5.10}$$

and the mirror-image responses are the $n = \pm 1$ terms,

$$\begin{aligned} X_{im}(f) = {} & \frac{f_s}{2} X_c\left(f - \frac{f_s}{2}\right)[1 - e^{j2\pi f \Delta_e} e^{-j\pi \Delta_e f_s}] + \\ & \frac{f_s}{2} X_c\left(f + \frac{f_s}{2}\right)[1 - e^{j2\pi f \Delta_e} e^{j\pi \Delta_e f_s}] \ . \end{aligned} \tag{5.11}$$

From (5.10) and (5.11) it can be determined that if the input signal, $x_c(t)$, is a unity-amplitude sinusoid with frequency f_x, then the output spectrum consists of the desired component at f_x and a mirror image at $f_s/2 - f_x$. This is illustrated in Figure 5.6. The timing-related image-rejection ratio, $IR_{\Delta e}$, is defined as the ratio of the signal power at f_x to the image power at $f_s/2 - f_x$:

$$\begin{aligned} IR_{\Delta e} = \frac{P_{sig}}{P_{im}} &= \frac{2 \times (f_s^2/4)}{2 \times (f_s^2/16) \times \left|1 - e^{j2\pi(f_s/2 - f_x)\Delta_e} e^{-j\pi \Delta_e f_s}\right|^2} \\ &= \frac{4}{\left|1 - e^{j2\pi(f_s/2 - f_x)\Delta_e} e^{-j\pi \Delta_e f_s}\right|^2} \ . \end{aligned} \tag{5.12}$$

If the input signal frequency, f_x, is approximately $f_s/4$ and $\Delta_e << 1/f_s$, then (5.12) simplifies to

$$IR_{\Delta e} \approx \frac{16}{\pi^2 \Delta_e^2 f_s^2} \ . \tag{5.13}$$

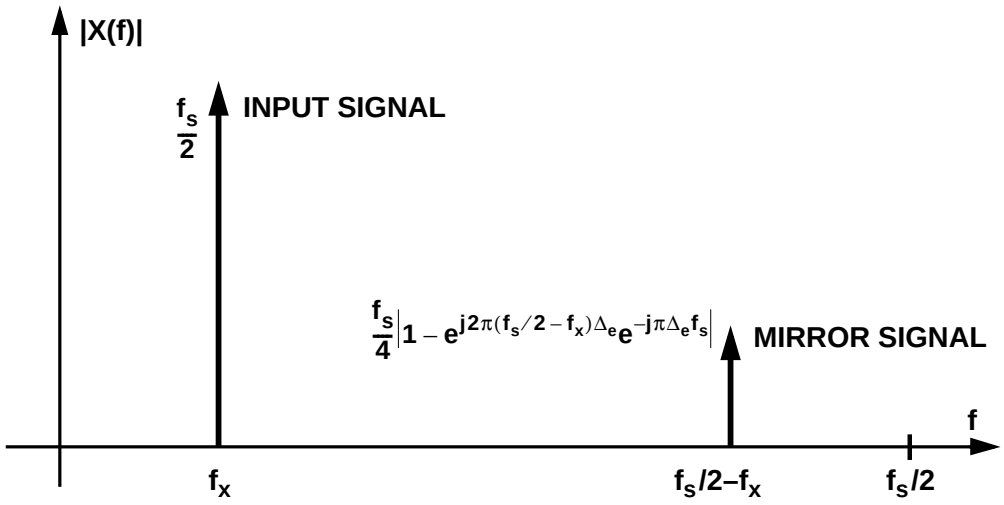
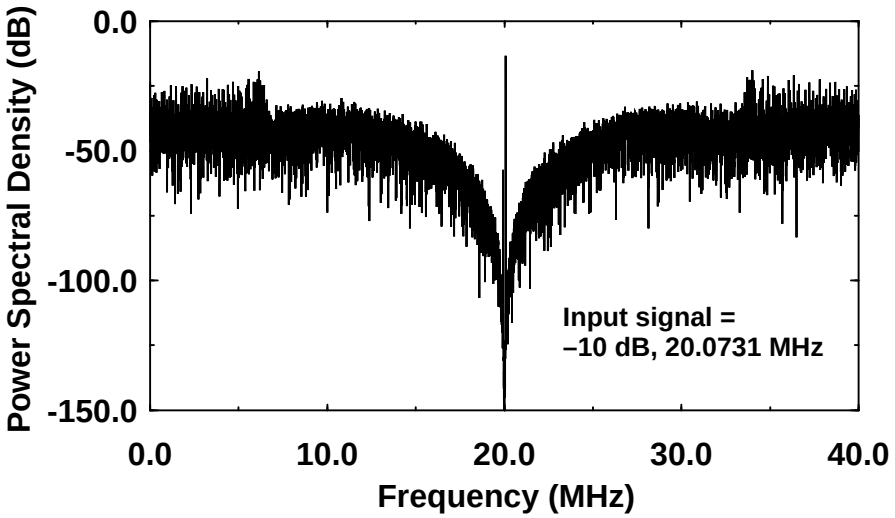


Figure 5.6: Output spectrum of a sampled sinusoid with frequency f_x and unity amplitude when the sampling time is perturbed for every other sample by Δ_e. Spectrum is symmetric around dc.

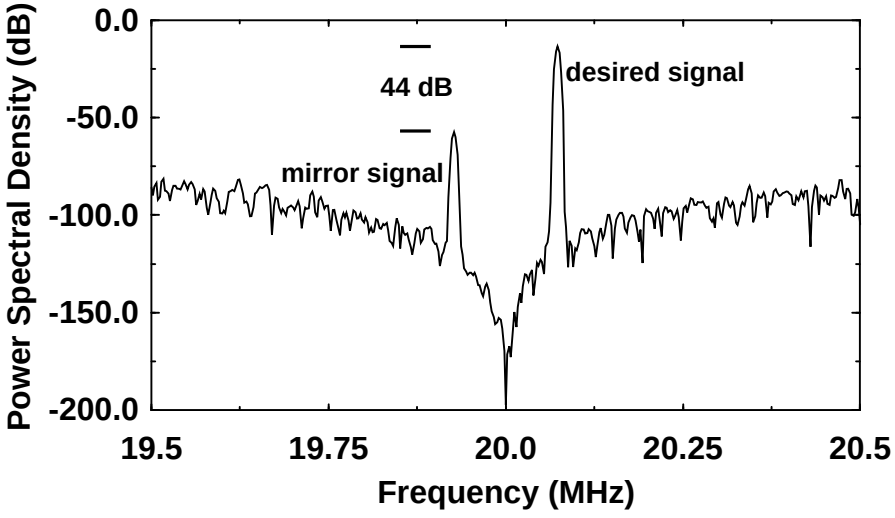
As an example, for a sampling frequency of 80 MHz, an input sinusoid frequency of 20 MHz + f_{IF} (where f_{IF} << 20 MHz), and a systematic timing error of 100 ps, (5.13) predicts that the mirror signal at 20 MHz – f_{IF} is suppressed by 44 dB with respect to the input signal. Since this mirror signal is present at the front-end of the two-path modulator, it is shaped by the same transfer function as the input signal. Therefore, at the two-path modulator's output, the suppression of the timing-related image will also be 44 dB. This is confirmed in Figure 5.7, which shows the simulated output spectrum of an $f_s/4$ modulator using two-path resonators. The input signal frequency is 20 MHz + 73.1 kHz and the systematic timing error, Δ_e, is 100 ps. As predicted, the image at 20 MHz – 73.1 kHz is suppressed by 44 dB.

5.3 Two-Path Modulator Block Diagram

The proposed two-path implementation for the fourth-order, $f_s/4$ modulator of Figure 4.1 is shown in Figure 5.8. The modulator consists of two resonators employing the two-path



(a)



(b)

Figure 5.7: (a) Output spectrum of the proposed two-path modulator with a systematic timing error, Δ_e, of 100 ps, and (b) a zoomed-in view of the passband centered around $f_s/4$.

topology described in Section 5.2, followed by a comparator that serves as the 1-b quantizer and a two-level (1-b) D/A converter. The modulator is controlled by two-phase, non-overlapping clocks. During Φ_1, the outputs of one set of highpass path filters are sam-

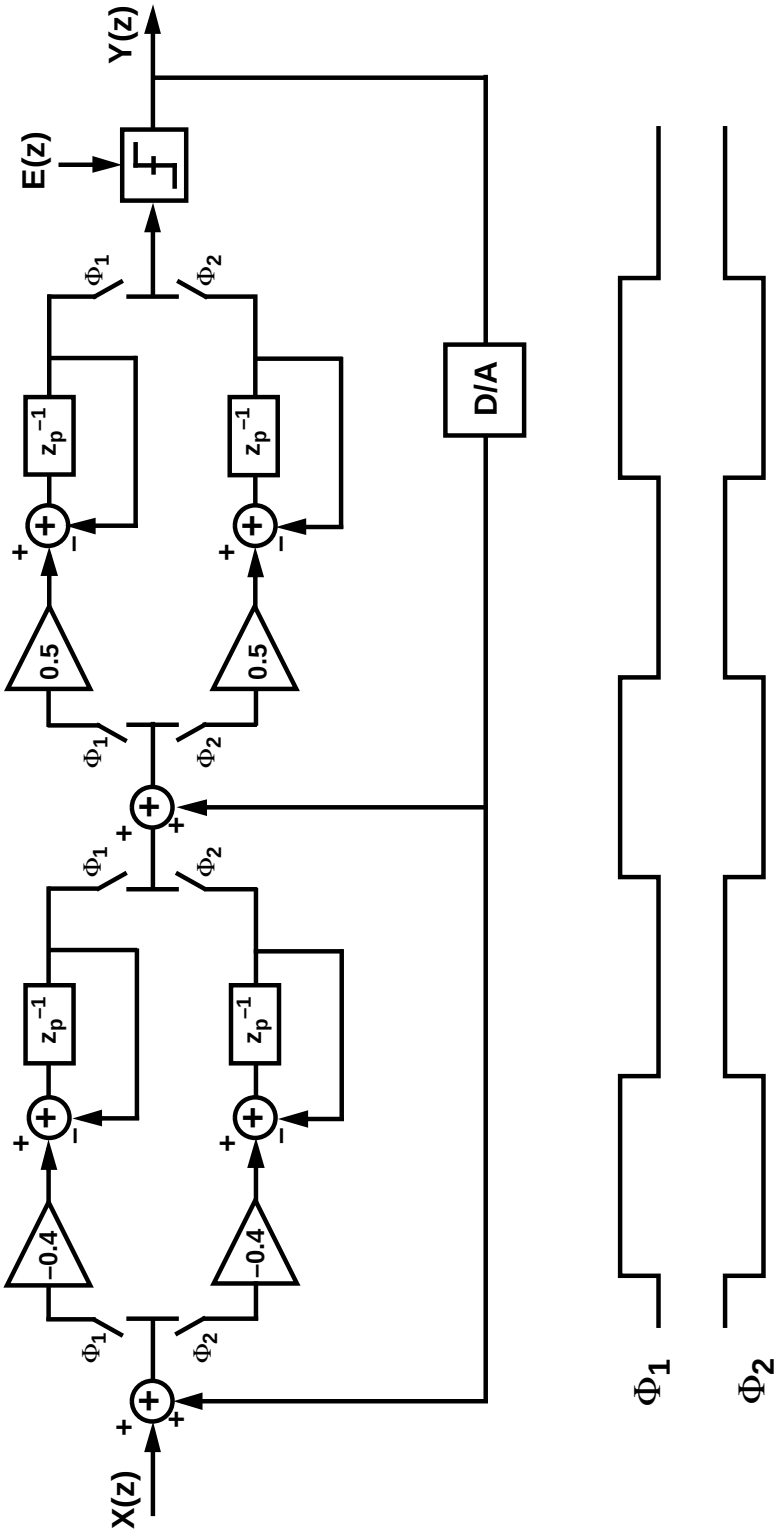


Figure 5.8: Fourth-order bandpass modulator implemented using two-path resonators.

pled, while on Φ_2, the outputs of their counterparts are sampled. The quantizer is clocked on both Φ_1 and Φ_2; thus, the sampling rate for the overall modulator is twice that of each path filter.

5.3.1 Two Interleaved Highpass Modulators

In a switched-capacitor implementation of the proposed two-path modulator, the summation of the resonator input signal with the quantizer feedback can be merged into the constituent path filters of each resonator. Upon redrawing the block diagram to reflect this fact, Figure 5.9 shows that the experimental bandpass modulator is essentially comprised of two independent, interleaved highpass modulators that are clocked 180° out of phase with each other. Also, in Figure 5.9 the single 1-b quantizer in Figure 5.8 has been partitioned into two independent 1-b quantizers. It is important to note that the total quantization noise power in the modulator of Figure 5.9 is not doubled by the presence of two quantizers because the quantizers are clocked on alternate clock cycles and the outputs of the two paths are interleaved, not summed.

If the two quantizers are identical, then the output from the modulator in Figure 5.9 is identical to the case where only a single quantizer is used. Although it is not necessary to partition the quantizer in this manner, the use of separate quantizers allows for a more modular design and simpler layout. Two independent quantizers were used in the experimental prototype.

Offsets in the comparators can potentially generate out-of-band tones in the output spectrum. If the offsets in the comparators of Figure 5.9 are identical, then the effect is equivalent to having a dc offset in the comparator of a single-path modulator. In this case, as explained in Section 4.1.4, dc tones can be generated in the output spectrum of the modulator. If the offsets in the two comparators are mismatched, then tones can be generated at $f_s/2$ as well as dc. This effect is illustrated in Figure 5.10 for the case when one comparator has an offset of $\Delta/40$, and the other comparator has an offset of $-\Delta/40$; Δ is the step size of the two-level quantizer. Intuitively, the presence of a tone at $f_s/2$ is understood

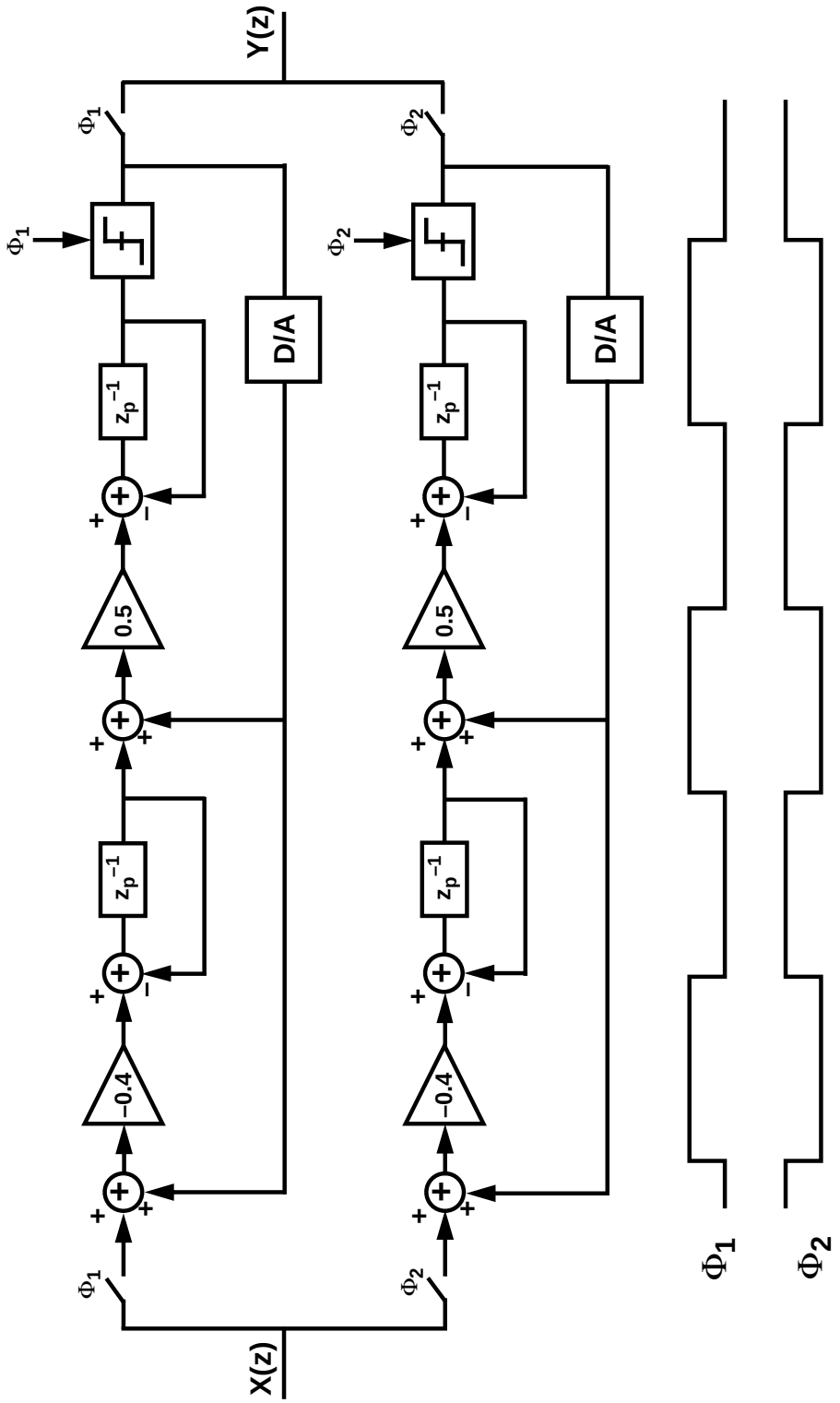


Figure 5.9: Partitioning of bandpass modulator into two independent highpass paths.

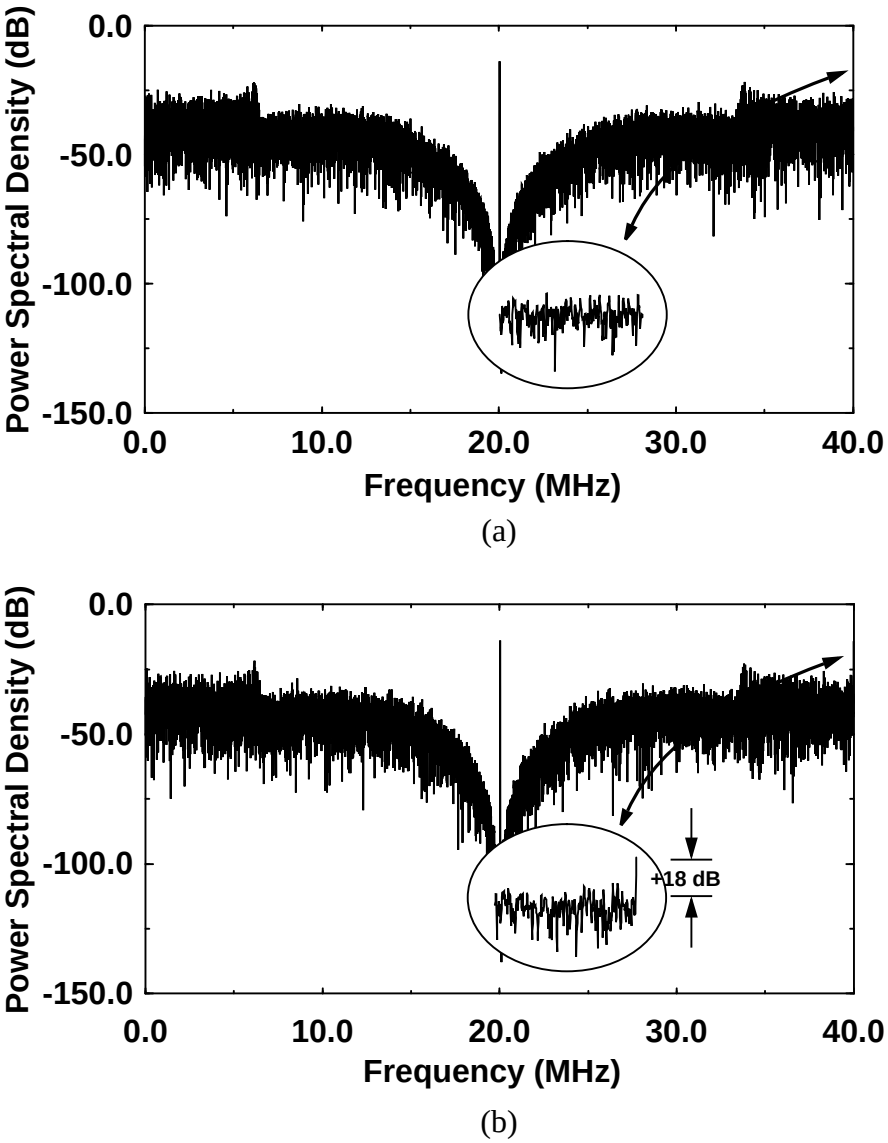


Figure 5.10: Output spectrum with a close-up view around dc when (a) both comparators do not have an offset, and (b) one comparator has an offset of $\Delta/40$ and the other has an offset of $-\Delta/40$; $\Delta = 1$ V.

by noting that each individual comparator is clocked at $f_s/2$. Therefore, a mismatch between the offsets of the two comparators can be viewed as the injection of an error signal with frequency $f_s/2$ into the input of one comparator. Since the magnitude of the noise transfer function of the proposed $f_s/4$ modulator is a maximum at dc and $f_s/2$, the tones

due to offset are not suppressed by the feedback in the modulator. However, aside from compressing the dynamic range of the modulator, the net effect of these offset-related tones should be negligible if they do not fall into the passband as a result of mixing with the signal at $f_S/4$ through circuit-related nonlinearities.

To the extent that the quantizers are not perfectly matched, there will also be an equivalent gain and phase error between the transfer functions of the two paths, thus contributing to the incomplete suppression of the mirror-image signal. However, this effect is likely to be small in comparison with mismatch in the front-end path filters because the image signal introduced at the quantizer is shaped by the same fourth-order noise transfer function that attenuates the quantization noise. This effect is illustrated in Figure 5.11, which illustrates the spectrum near $f_S/4$ when the two paths are identical except for a 125 mV mismatch between the two comparator thresholds. An inband image is introduced in both cases, but it can be seen that the image suppression becomes poorer as the input moves further away from the center of the passband around 20 MHz.

5.3.2 Stability in the Two-Path Modulator

The fact that the modulator of Figure 4.1 can be partitioned into a two-path system has interesting stability implications because each of the two paths are only second-order systems that do not share state information. Therefore, although the overall architecture of the proposed modulator is a fourth-order feedback system, it is not as susceptible to instability, as are the generalized fourth-order noiseshapers described in Section 3.3.4. It is notable that the proposed $f_S/4$ architecture degenerates cleanly into two independent highpass modulators precisely because the architecture was derived via the dc-to-$f_S/4$ transformation, (3.23), which maps z^{-1} to $-z^{-2}$. This degeneracy is not necessarily preserved if the modulator architecture is designed using the generalized filter approach, which focuses on the zeros and the out-of-band gain of the noise transfer function. It is possible to synthesize alternative stable, higher-order f_S/X architectures using various z^{-1} to $\pm z^{-N}$ transformations, such as the sixth-order $f_S/6$ modulator described in Chapter 8, but a comprehensive exploration of these architectures was not pursued in this work.

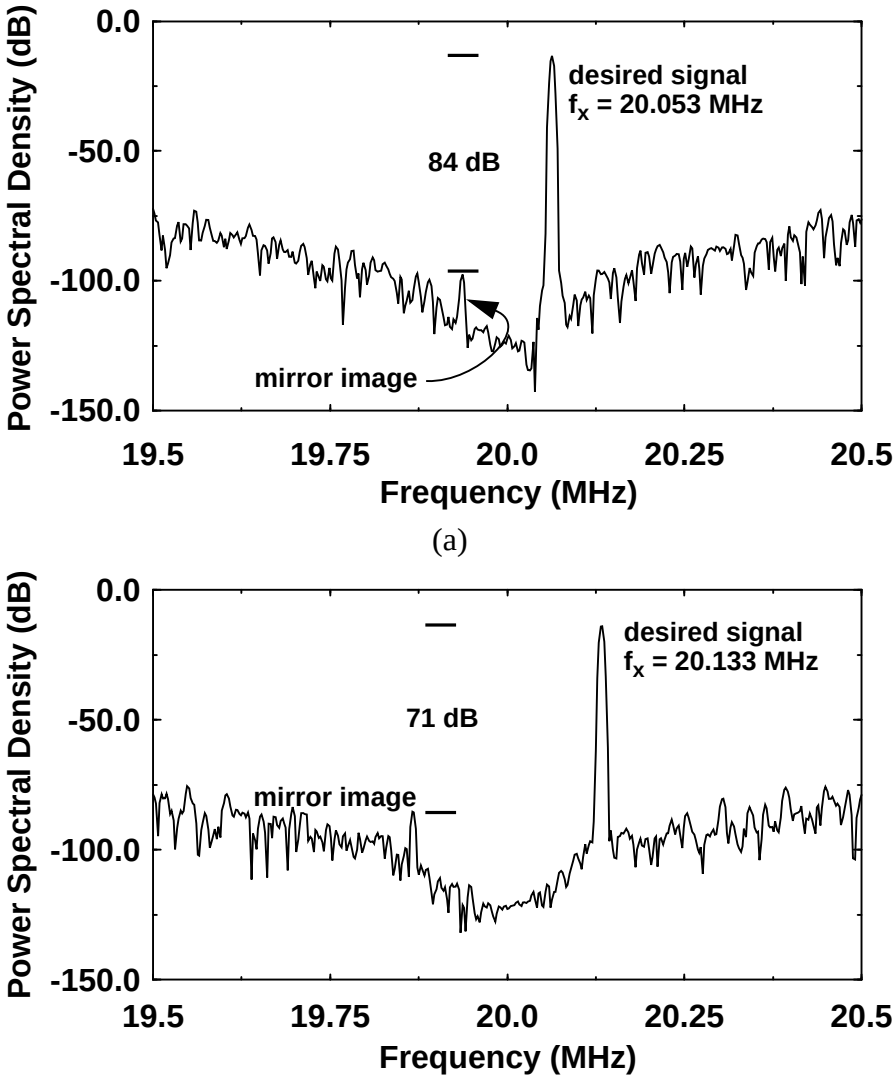


Figure 5.11: Inband image that is introduced by comparator mismatch in the two-path modulator for input signal frequencies, (a) f_x = 20.053 MHz, and (b) f_x = 20.133 MHz.

Although the two-path $f_s/4$ modulator has the dynamic behavior of a second-order system, it cannot be claimed that it is inherently stable simply because its architecture is derived from a stable, second-order lowpass modulator. The stability of the two-path $f_s/4$ modulator is sensitive to specific implementation issues in a manner that is not reflected in

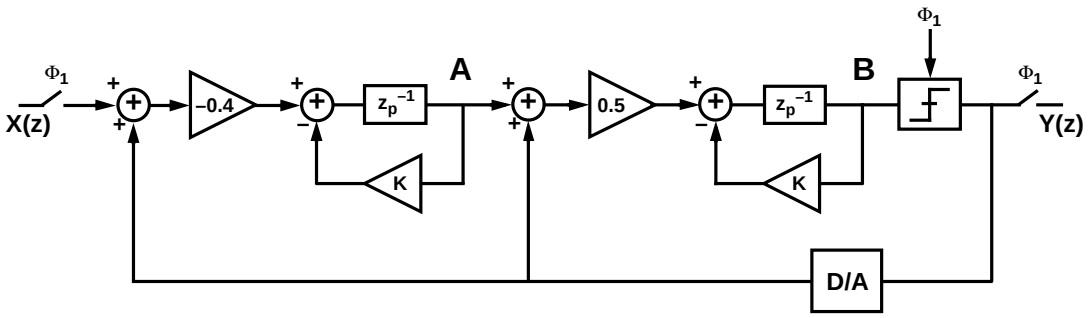


Figure 5.12: One path of the proposed modulator with capacitor mismatch errors in the path filters reflected in the feedback factor, *K*. The internal states of the path are denoted *A* and *B*.

lowpass modulators. Consider the block diagram of one path of the two-path modulator illustrated in Figure 5.12. The transfer function of each of the path filters is

$$H(z) = \frac{z^{-1}}{1 + Kz^{-1}} . \tag{5.14}$$

Ideally, the feedback coefficient of each path filter, *K*, is 1, but in practice, *K* is often less than 1 due to finite amplifier gain. However, depending on the particular switched-capacitor circuit topology that is chosen, capacitor mismatch can also cause *K* to be slightly greater than one. In this case, the pole of the highpass path filter will lie outside of the unit circle, $|z| = 1$, which means that the path filter is inherently unstable. Depending on the severity of the path filter pole error and the magnitude of the initial state and overload input that the modulator is subjected to, an instability may be induced in the modulator that persists after the input to the modulator has been removed. This instability is characterized by internal states that continue growing without bound, or that clip at internal limits, even when there is no input to the modulator.

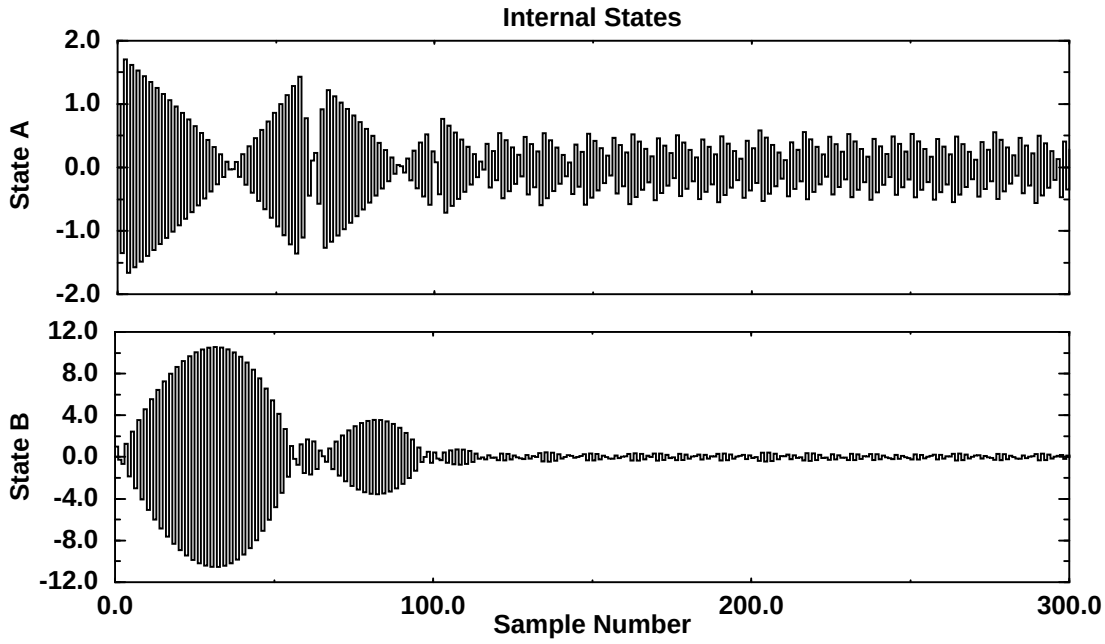
Stability in the proposed two-path modulator was assessed with extensive behavioral simulations of the single path depicted in Figure 5.12. The internal states of the path, which are the outputs of the first- and second-stage path filters, are denoted *A* and *B* respectively. The error factor, *K*, was swept from 0.97 to 1.03 and *A* and *B* were preloaded

with different overload conditions. For the case when $K = 1.01$ and A and B are preloaded to $5 \times |V_{ref}/2|$, where $|V_{ref}/2|$ is the magnitude of the feedback reference levels, it can be seen in Figure 5.13(a) that the modulator is stable because the internal states subside after an initial transient period; the inband SNR is also consistent with that predicted by linear analysis. However, for the case depicted in Figure 5.13(b), when $K = 1.02$ and A and B are again preloaded to $5 \times |V_{ref}/2|$, the modulator is clearly unstable; the states continue growing until they are artificially clipped in the simulation. The relationship between capacitor mismatch in the switched-capacitor circuit and the error feedback factor, K, in the block diagram is determined by the specific circuit topology chosen and will be discussed in the following chapter.

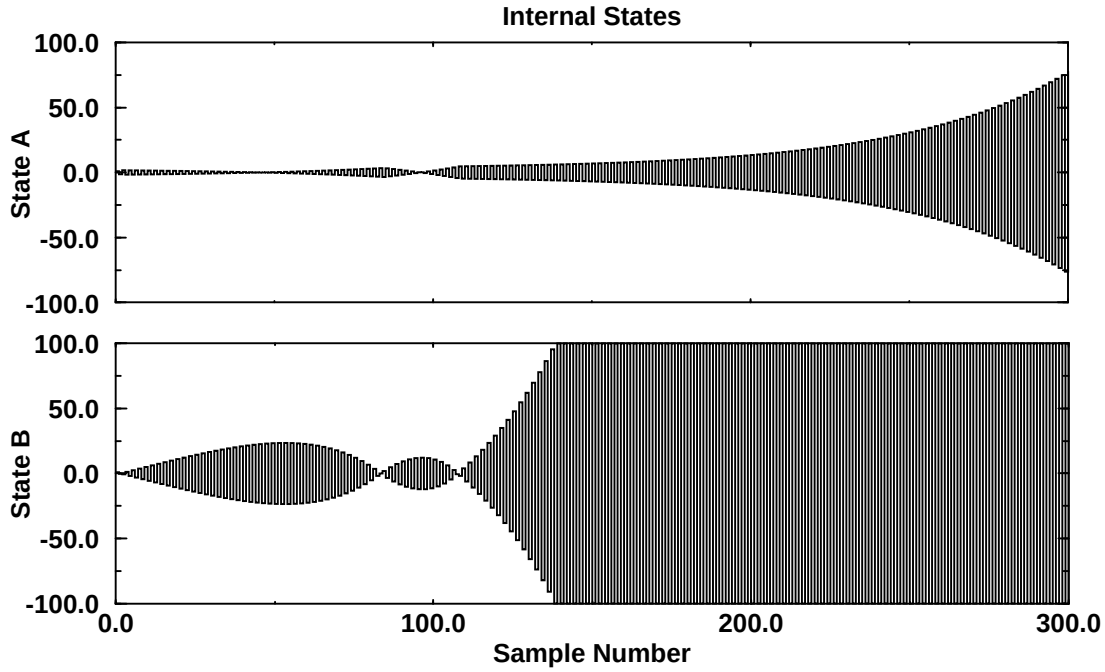
5.4 Summary

In this chapter, the essential relationships for N-path filters were reviewed, and it was shown that the resonators of the proposed, fourth-order, $f_s/4$ modulator can be implemented easily by interleaving two highpass filters. The nonidealities of the two-path resonator were explored within the context of the bandpass modulator. It is seen that path mismatch leads to an image of the desired signal produced at a mirror frequency centered around $f_s/4$. This is analogous to the image that is produced by phase and gain errors during analog I and Q demodulation. Systematic timing errors that result in nonuniform sampling of the input signal also result in incomplete image suppression.

It was also shown that it is possible to partition the modulator into two independent second-order paths. The stability of the modulator is then seen to be governed by second-order dynamics. However, if the path filters that comprise the modulator are unstable because of implementation nonidealities, it is possible to excite the modulator into an unstable state that is characterized by large oscillations in internal states and a poor inband SNR that is not commensurate with that predicted by linear analysis. The potential for the onset of instability is related to the initial conditions in the modulator as well as the magnitude of the error resulting from circuit nonidealities such as capacitor mismatch.



(a)



(b)

Figure 5.13: The internal states, *A* and *B*, of one modulator path that is subjected to a recovery test. *A* and *B* are preloaded to $5 \times |V_{ref}|$ and the feedback factor, *K*, is equal to (a) 1.01 and (b) 1.02. The input signal amplitude is –3 dB relative to $V_{ref}/2$.

Fortunately, behavioral simulations indicate that the modulator remains stable for a wide range of overload conditions provided that the pole error in the path filters remains bounded by approximately 1%. In the following chapter, it is shown that this condition requires capacitor matching on the order of 1% (which can readily be achieved) for the specific circuit topology chosen to implement the path filter.

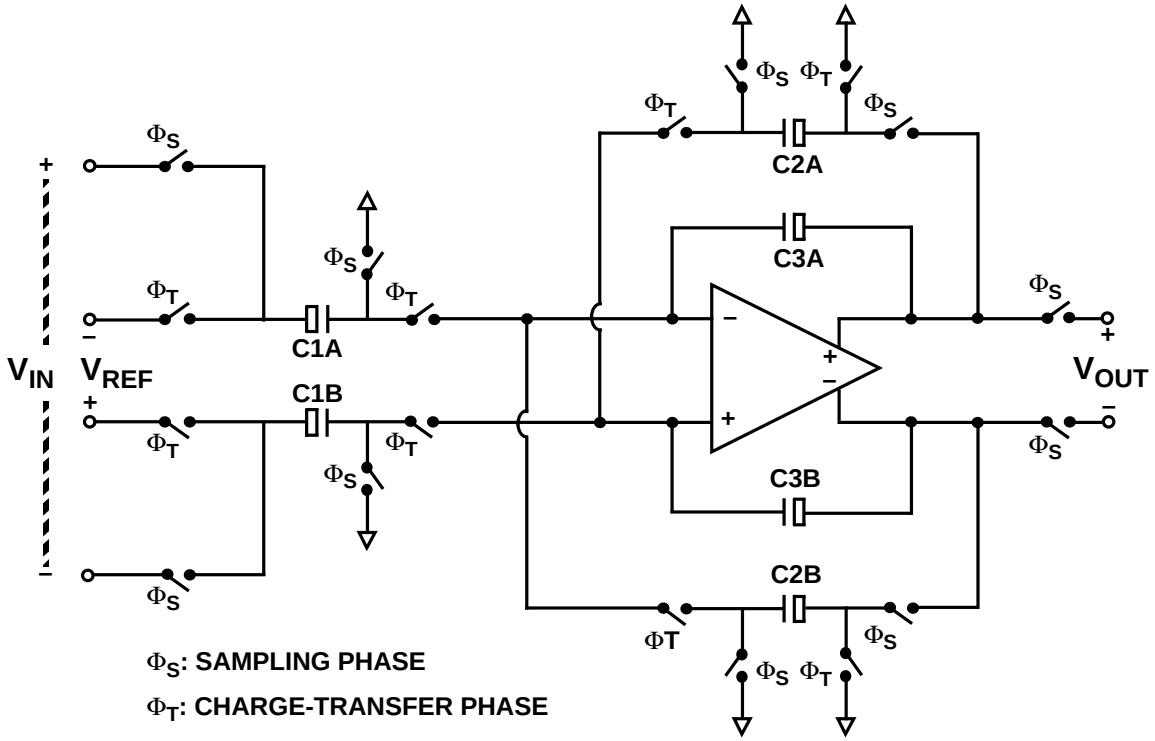
Chapter 6 *Implementation*

This chapter describes the design and implementation of an $f_s/4$ bandpass modulator that utilizes the two-path architecture proposed in Chapter 5. The objective of this design is to demonstrate the feasibility of implementing a modulator with an effective sampling frequency as high as 80 MHz and a dynamic range exceeding 70 dB for a 200-kHz passband centered at $f_s/4$. For this oversampling ratio, the fourth-order architecture is designed to suppress inband quantization noise by a large margin with respect to the noise floor set by electronic noise.

The experimental modulator has been integrated in a 0.6-μm, single-poly, triple-metal CMOS technology. This technology does not include a high-density, linear capacitor option such as double-poly or poly-diffusion capacitors. Therefore, the capacitors were implemented using the capacitance between metal interconnect layers. This results in a substantial power dissipation penalty because of the large parasitics associated with the capacitor structures. For this reason, power dissipation in the prototype was only loosely constrained to be less than 100 mW when the modulator is operated from a 3.3-V supply. Substantial power savings should be possible in a technology with a smaller bottom-plate parasitic capacitance.

6.1 Switched-Capacitor Highpass Path Filter

As described in Section 5.3, the proposed two-path modulator is comprised of $f_s/4$ resonators that are implemented using two interleaved highpass filters, each with the path transfer function



Capacitor	Stage 1	Stage 2
C1A, C1B	300 fF	200 fF
C2A, C2B	1.5 pF	800 fF
C3A, C3B	750 fF	400 fF

Figure 6.1: Fully-differential, switched-capacitor implementation of the highpass path filter with capacitor values for the first- and second-stage filters.

$$H(z_p) = G \cdot \frac{z_p^{-1}}{1 + z_p^{-1}} . \tag{6.1}$$

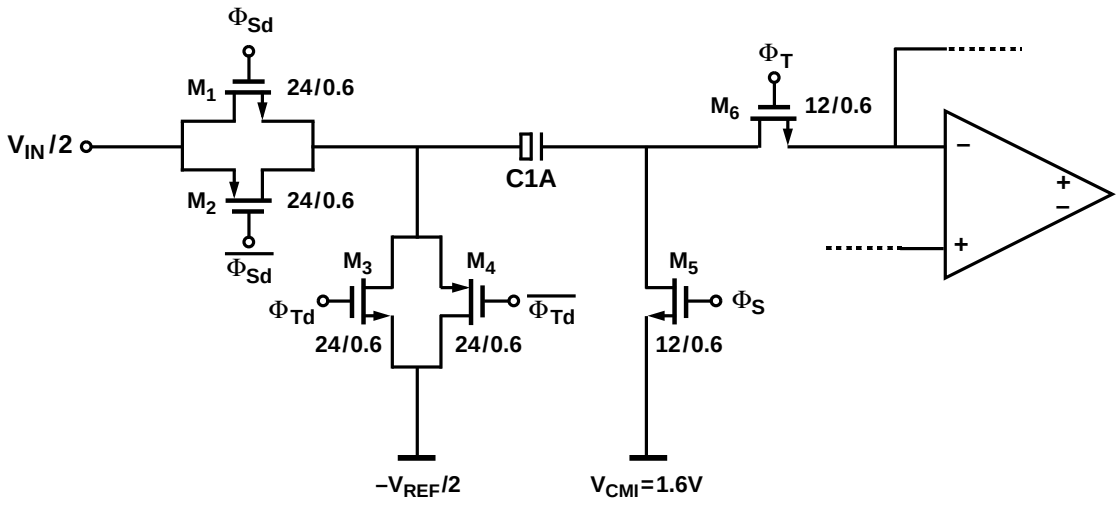
The highpass path filters are implemented using the fully-differential, switched-capacitor circuit shown in Figure 6.1. The bottom plates of the capacitors are denoted with rectan-

gles to emphasize the significance of the large bottom-plate parasitic that is inherent in the capacitor structure.

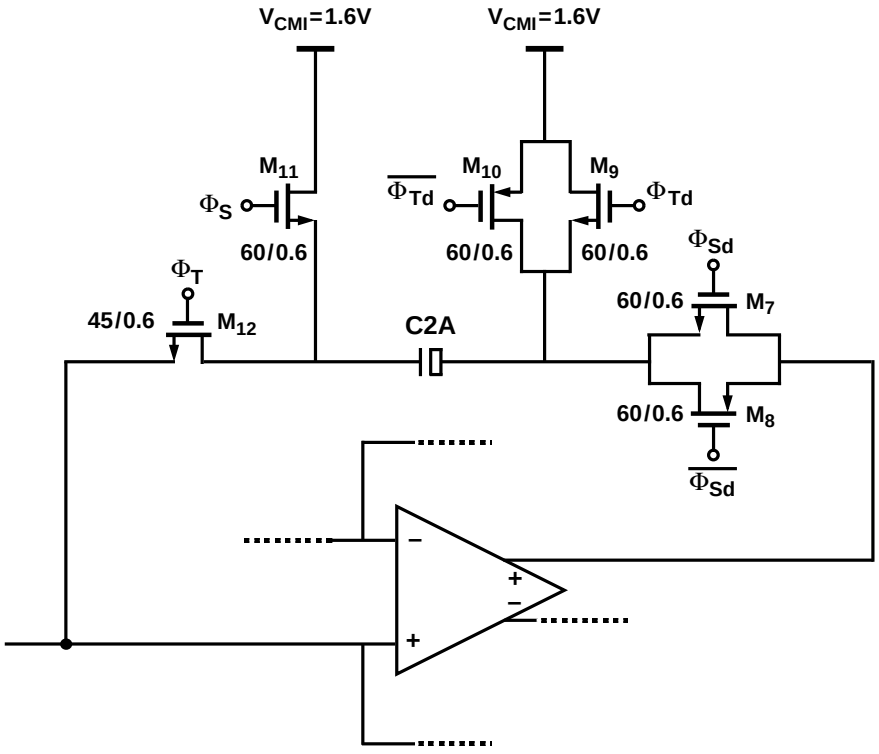
The differential filter topology used in the circuit of Figure 6.1 ensures that common-mode disturbances such as noise from the power and ground rails, as well as signal-independent switch charge injection, will be cancelled to the first order [93]. Furthermore, the signal voltage swings are effectively doubled, which increases the maximum signal power by a factor of four, while the kT/C noise power is only increased by a factor of two. Thus, a net improvement of 3 dB in the peak SNR is obtained if the noise floor of the circuit is governed by kT/C noise. If op amp noise dominates the noise performance of the fully-differential circuit, the result is a 6 dB improvement in SNR [93]. However, these advantages are tempered by the additional complexity imposed by the need for common-mode feedback circuitry in the amplifier and the greater area required to implement a fully-differential topology.

The switches used in the filter of Figure 6.1 are shown in more detail in Figure 6.2. Transmission gates comprised of *n*- and *p*-transistors in parallel are utilized at the nodes that experience a large voltage swing to ensure that the switch remains conducting throughout the entire signal excursion. Otherwise, at the extremes of the swings at these nodes, the switch may have an undesirably large *on* resistance, or may even turn off. The switches connected to the operational amplifier input terminals are implemented using NMOS devices only because these nodes remain close to the input common-mode voltage, V_{CMI}, which ideally remains constant. In the experimental prototype, V_{CMI} is set to 1.6 V.

The switches in Figure 6.2 are controlled by two non-overlapping clock phases, Φ_S and Φ_T, and delayed phases, Φ_{Sd}, Φ_{Td}, $\overline{\Phi_{Sd}}$, $\overline{\Phi_{Td}}$. The use of both primary and delayed clock phases to control the switch network guarantees that the switches tied to dc common-mode voltages are turned off prior to the switches connected to nodes that experience large signal-dependent swings. For example, during the sampling phase, Φ_S, M_5 and M_{11}, which are tied to V_{CMI}, are turned off prior to switches M_1/M_2 and M_7/M_8, thereby avoiding signal-dependent charge injection onto the sampling capacitors, $C_{1A,B}$ and $C_{2A,B}$ [94].



(a)



(b)

Figure 6.2: Switch networks used to sample the (a) input signal and (b) output of the amplifier in the highpass path filter. Transistor sizes are in μm.

Similarly, during the charge-transfer phase, Φ_T, the switches connected to the op amp input terminals, M_6 and M_{12}, are turned off before switches M_3/M_4 and M_9/M_{10} to insure that the charge injected onto the integration capacitors, $C_{3A,B}$, is, to first order, independent of the signal.

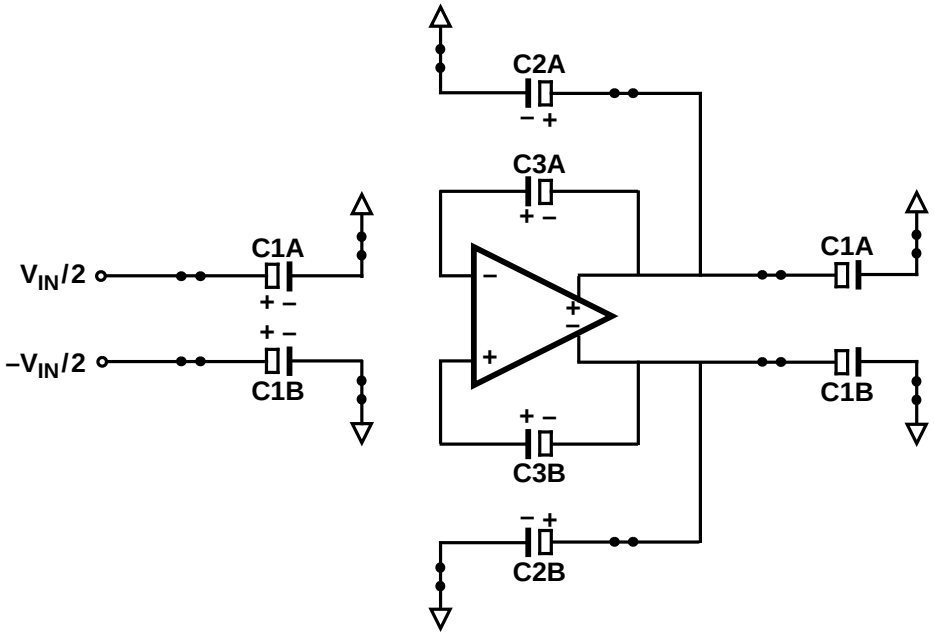
6.1.1 Filter Operation

The filter operation during the sampling and charge-transfer phases is depicted in Figure 6.3. On the sampling phase, Φ_S, a charge proportional to V_{IN} is stored on C_{1A} and C_{1B}, and a charge proportional to V_{OUT} is stored across C_{2A} and C_{2B}. On the subsequent charge-redistribution phase, Φ_T, $-V_{REF}$ is sampled onto $C_{1A,B}$, and charge is transferred from C_{1A} to C_{3A}, C_{1B} to C_{3B}, C_{2A} to C_{3B}, and C_{2B} to C_{3A}. Because the capacitors C_{2A} and C_{2B} are cross-coupled around the operational amplifier, the charge transferred from C_{2A} and C_{2B} effectively undergoes an inversion during the charge-redistribution phase. In the z-domain, the output of the highpass path filter is thus

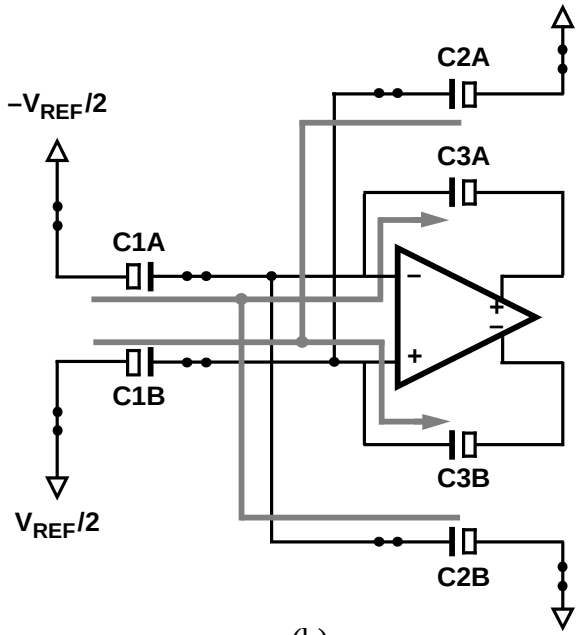
$$V_{OUT}(z_p) = \frac{C_{1A}}{C_{3A}} \times \frac{z_p^{-1}}{1 + \left(\frac{C_{2B}}{C_{3A}} - 1\right) z_p^{-1}} \times (V_{IN}(z_p) + V_{REF}(z_p)) \tag{6.2}$$

where, as explained in Section 5.1, z_p^{-1} denotes a single delay with respect to the path sampling frequency. When $C_{2B,A} = 2 \times C_{3A,B}$, the path filter realizes the desired highpass transfer function of (6.1).

The sampling and charge-transfer phases of the path filter can be related to the operation of the proposed, two-path bandpass modulator by referring to the timing diagram depicted in Figure 5.9. It is seen that the Φ_1 path, which can be regarded as one of two independent parallel modulators with interleaved outputs, samples the input, *X(z)*, on phase Φ_1 and redistributes charge on phase Φ_2, whereas the Φ_2 path operates 180° degrees out of phase with the Φ_1 path, sampling the input on phase Φ_2 and redistributing charge on phase Φ_1.



(a)



(b)

Figure 6.3: Switched-capacitor highpass path filter configured during the (a) sampling phase, Φ_S, and (b) charge-redistribution phase, Φ_T.

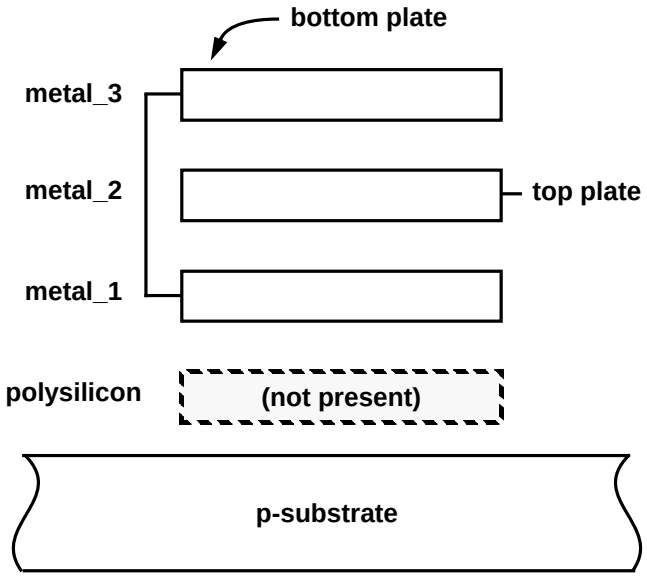


Figure 6.4: Metal sandwich capacitor implementation.

6.1.2 Capacitor Sizing

Because no explicit analog capacitor option was available in the 0.6-μm, single-poly, triple-metal CMOS technology used to implement the experimental modulator, the capacitors were synthesized from metal 3–metal 2–metal 1 stacks as depicted in Figure 6.4. In this technology, the capacitance per unit area of a stacked-metal structure is only on the order of 0.074 fF/μm^2, and the bottom-plate parasitic capacitance is estimated to be 70% of the nominal capacitance value. The capacitance per unit area could be increased to approximately 0.130 fF/μm^2 by including polysilicon in the stack such that the top plate is comprised of metal 3–metal 1 and the bottom plate is comprised of metal 2–poly. However, the bottom-plate parasitic capacitance then increases to an estimated 80% of the nominal capacitance value. This was deemed to be an unacceptable tradeoff. Although the transfer characteristic of the path filter topology shown in Figure 6.1 is parasitic-insensitive, bottom-plate capacitances increase the capacitive load that the operational amplifiers must drive, thereby increasing the power dissipation if the unity-gain bandwidth of the

amplifier is to remain constant. In this technology, it is imperative to keep the size of the capacitors as small as allowed by kT/C noise and matching considerations.

With the preceding considerations in mind, the input sampling capacitors in the first stage, $C_{1A,B}$, were sized at 300 fF. The feedback capacitors, $C_{3A,B}$, are governed by the desired resonator gain, $C_{1A,B}/C_{3A,B}$, and the output sampling capacitors, $C_{2A,B}$, are determined by (6.2) to be twice the value of $C_{3A,B}$. Smaller capacitors can be used in the filters comprising the second stage of the proposed, two-path modulator because of relaxed requirements with respect to kT/C noise and capacitor mismatch as compared to the first-stage filters. Errors introduced after the first stage of the modulator are attenuated by noiseshaping in addition to oversampling [14]. Thus, sampling capacitors of the second stage were scaled to 200 fF to reduce the loading on both the first and second-stage operational amplifiers.

6.1.3 Switch Noise

Two noise sources intrinsic to the MOS switches, thermal noise and flicker noise, can potentially perturb the filter operation. Thermal noise is associated with the random motion of carriers in the resistive channel, and flicker ($1/f$) noise is associated with flow of direct current in the device. In the analysis of switch noise below, $1/f$ noise is considered negligible because it is assumed there is no static current flowing through the switched capacitors, and hence, none through the MOS device [95].

The thermal noise contributed by the MOS switches in the path filter can be estimated by modeling each switch path with the sample-and-hold circuit shown in Figure 6.5. When Φ_S is high and the MOS switch is on, the channel is modeled as a noiseless resistor, R_{ON}, in series with a noise source, e_R, that has a power spectral density

$$S_R(f) = 4kTR_{ON} \quad , \qquad 0 < f < \infty \tag{6.3}$$

where k is Boltzmann's constant and T is absolute temperature. The variance of the noise sampled onto capacitor C_S is determined by integrating the noise power spectral density,

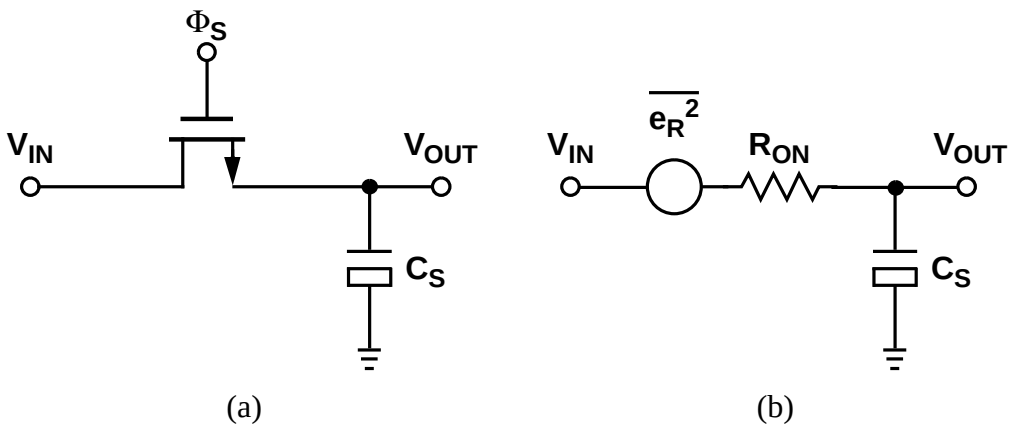


Figure 6.5: (a) MOS sample-and-hold, and (b) its equivalent noisy circuit when Φ_S is high.

$S_R(f)$, shaped by $|H(f)|^2$, where $H(f)$ is the transfer function of the lowpass filter comprised of R_{ON} and C_S:

$$\overline{e_{out}^2} = \int_0^\infty (4kTR_{ON}) \frac{df}{1 + (2\pi f R_{ON} C_S)^2} = \frac{kT}{C_S} . \tag{6.4}$$

Since the path filter sampling frequency, f_{ps}, is much lower than the circuit bandwidth set by R_{ON} and C_S, it can be shown that the process of sampling the switch noise results in the concentration of the total noise power kT/C_S into the path sampling bandwidth, $-f_{ps}/2$ to $f_{ps}/2$ [85].

In the proposed implementation of the highpass path filter, it can be seen in Figure 6.3(a) that during the sampling phase, switch noise is sampled onto capacitors C_{1A}, C_{1B}, C_{2A}, and C_{2B}. During the charge-transfer phase, additional noise is sampled when the charge from capacitors C_{1A}, C_{1B}, C_{2A}, and C_{2B} is transferred to the integration capacitors, C_{3A} and C_{3B}. Since the noise sources are uncorrelated, their powers add. Therefore, using the capacitor values for the first-stage highpass filter, the total power of the switch noise referred to the filter input is

$$\overline{e_{switch}^2} = kT\left(\frac{2}{C_{1A}} + \frac{2}{C_{1B}} + \frac{2}{C_{2A}} + \frac{2}{C_{2B}}\right) \tag{6.5}$$

$$= 1.38 \times 10^{-23} JK^{-1} \cdot 300K \cdot \left(\frac{2}{300\,fF} + \frac{2}{300\,fF} + \frac{2}{1.5\,pF} + \frac{2}{1.5\,pF}\right)$$

$$= 6.624 \times 10^{-8} V^2 .$$

In this expression, the factor of 2 accounts for the fact that noise is sampled during both the sampling and charge-transfer phases, and it has been assumed that the noise sampled during both phases is bandlimited by the switch resistance and the sampling capacitor. This assumption results in an overestimate of the noise contribution during the charge-transfer phase because the charge-transfer process is actually bandlimited by the operational amplifier, not by the switch network, as was assumed in the derivation of (6.4) [96], [97].

6.1.4 Amplifier Noise

In addition to kT/C noise from the switches, noise from the operational amplifier also degrades the performance of the filter. In the following analysis, it is presumed that all noise sources within the amplifier can be referred to a source at the amplifier's non-inverting input, denoted e_{amp} in Figure 6.6. The analysis is simplified by using a single-ended representation of the filter, but no error is inherent in this simplification because e_{amp} is defined to equal the input-referred noise of the actual amplifier used in the fully-differential filter. Capacitor C_2 is chosen to be $2\times C_3$ to yield the desired highpass transfer function, as stated in Section 6.1.1. Capacitor C_1 is unspecified in the following analysis because it only affects the gain of the filter through the ratio C_1/C_3.

The input-referred amplifier noise spectral density, $S_{amp}(f)$, typically consists of a white noise component, which is characterized by a power spectral density that is constant with frequency, and a $1/f$ noise component that is inversely proportional to frequency. In the proposed highpass filter, $1/f$ noise can be neglected because it is concentrated in a narrow region around dc, which even in devices exhibiting high flicker noise levels, only

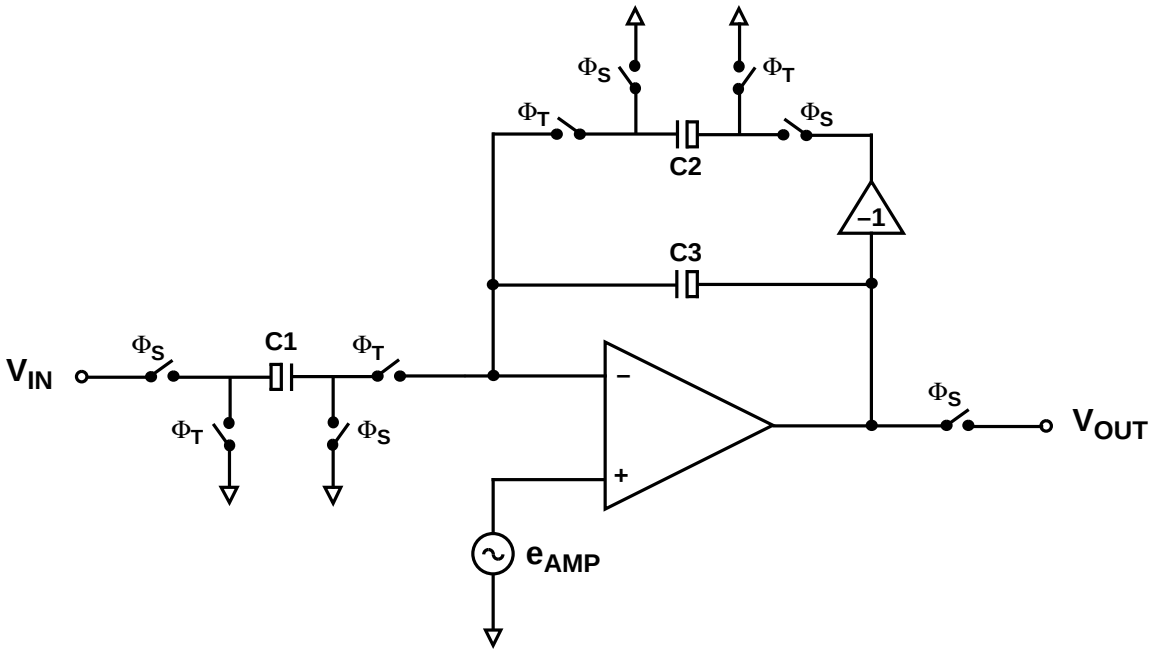


Figure 6.6: Single-ended representation of the proposed highpass path filter with an input, V_{IN}, and an input-referred amplifier noise source, e_{amp}.

extends into the MHz range [95], whereas the signal is centered at one-half of the path sampling frequency, $f_{ps}/2$. The input-referred amplifier noise power, $\overline{e_{amp}^2}$, is limited by the overall closed-loop bandwidth of the filter, which is largest during the sampling phase. Thus, it is conservatively assumed that the filter bandwidth during both phases, sampling and charge-transfer, is equal to the sampling-phase bandwidth. The total amplifier noise spectral density referred to the amplifier's non-inverting input can then be written as

$$S_{amp,\,tot}(f) = \frac{S_{amp}(f)}{1 + (f 2\pi\tau_{cl})^2} = \frac{S_o}{1 + (f 2\pi\tau_{cl})^2}, \qquad 0 < f < \infty \tag{6.6}$$

where S_o is the amplifier's white noise density, and τ_{cl} is the closed-loop settling time constant during the sampling phase. The input-referred amplifier noise power, $\overline{e_{amp}^2}$, is found by integrating $S_{amp,\,tot}(f)$ over all positive frequencies:

$$\overline{e_{amp}^2} = \int_0^\infty S_{amp,\,tot}(f)\,df = \int_0^\infty \frac{S_o}{1+(f2\pi\tau_{cl})^2}\,df = S_o \times \frac{1}{2\pi\tau_{cl}} \times \frac{\pi}{2}\ . \tag{6.7}$$

In this expression, the term $1/(2\pi\tau_{cl})$ is the –3 dB frequency in Hz of the filter when it is configured in the sampling phase. Therefore, (6.7) is consistent with the often used concept of a "noise bandwidth" of a circuit, which is equal to $\pi/2$ multiplied by the circuit's –3-dB frequency, f_{-3dB}, if that bandwidth is governed by a single-pole response [95]. Finally, as in the case of switch noise, it is assumed that as a result of sampling the amplifier noise, $\overline{e_{amp}^2}$ is distributed uniformly across the filter sampling bandwidth, $-f_{ps}/2$ to $f_{ps}/2$.

Insight into the influence of the amplifier's noise on the performance of the filter is gained by examining the terms involving e_{amp} in the time-domain difference equation that describes the filter:

$$v_o[n] + v_o[n-1] = \frac{C_1}{C_3}v_{in}[n-1] + \left(2+\frac{C_1}{C_3}\right)e_{amp}\left[n-\frac{1}{2}\right] + e_{amp}[n] - e_{amp}[n-1]\ . \tag{6.8}$$

A consideration of this expression reveals that the noise power is amplified at the output of the filter in two ways. First, (6.8) indicates that the power of the noise term $e_{amp}[n–1/2]$ is magnified by $(1+2C_3/C_1)^2$ with respect to the power of the input signal. This noise amplification factor can be large if the ratio of C_1/C_3 is less than one, as in the design of this modulator. A second, more subtle, effect is that a first-order differencing of e_{amp} is also referred to the input of the filter. In the frequency domain, a first-order differencing is equivalent to a first-order lowpass shaping function that has a zero at dc and a maximum at one-half of the filter sampling frequency, $f_{ps}/2$. This shaping is beneficial if the input signal is located near dc, as in a lowpass modulator. Unfortunately, in the proposed two-path modulator architecture, the signal passband is centered precisely at $f_{ps}/2$, where the shap-

ing function applied to the amplifier noise has its maximum amplitude. In other words, the amplifier noise is shaped to have a maximum spectral density in the desired passband.

The preceding discussion provides a qualitative feel for the noise behavior of the proposed highpass path filter with respect to the amplifier. However, it is difficult to quantitatively assess the impact of amplifier noise, e_{amp}, on the performance of the proposed two-path modulator by only considering the stand-alone filter. For example, it is known that amplifier noise in a switched-capacitor integrator with sampling capacitance C_S and integration capacitance C_I experiences a power gain of $(1+C_I/C_S)^2$ when it is referred to the input of the integrator [98]. If the integrator gain, C_S/C_I is small, the noise amplification factor can be substantial. However, when the integrator is embedded in the feedback loop of a lowpass ΣΔ modulator, a substantial fraction of the amplifier noise power experiences lowpass noiseshaping, which suppresses it in the signal band. This effect is not evident from a consideration of the integrator alone. A more complete description of this phenomenon in lowpass modulators can be found in [98]. An analogous shaping of the amplifier noise occurs in the proposed two-path $f_s/4$ modulator. Unfortunately, this shaping results in a noise gain from the amplifier to the output of the modulator, rather than a noise suppression as in the lowpass case. A detailed discussion of this effect is deferred until Section 6.3 when the noise of the entire two-path modulator is analyzed.

6.1.5 Filter Stability

A close consideration of (6.2) reveals the disturbing possibility that the highpass path filter will be unstable if the ratio C_{2B}/C_{3A} is greater than two. In that case, the path filter has a pole outside the unit circle, $|z| = 1$, indicating that the impulse response of the filter is unbounded and may saturate the filter, as well as the modulator, in the manner described in Section 5.3.2. Fortunately, for $C_{2B} = 2C_{3A}$, extensive behavioral simulations indicate empirically that the experimental modulator is stable if capacitor matching is good to at least 1%. With this level of matching, simulations show that the internal states of the modulator remain bounded under all non-overload conditions. Furthermore, the modulator recovers from being overdriven at the input, or when initially placed in an overload state.

In effect, the nonlinear feedback loop encompassing the unstable path filters and the 1-b quantizer drives the poles of the unstable filter back within the unit circle. With careful layout techniques, capacitor matching of 0.3% can be routinely achieved in modern CMOS processes, and matching as good as 0.1% has been observed [30]. Furthermore, in this design, the matching between capacitors is aided by the physically large areas needed to implement the desired capacitance values.

6.1.6 Effect of Finite Amplifier Gain and Bandwidth

Finite dc gain and bandwidth in the operational amplifier degrade the performance of the highpass path filter in a manner similar to the switched-capacitor integrator discussed in Section 4.2.1. It can be shown that with finite dc gain, *A,* the transfer function of the filter takes on the form

$$V_{OUT}(z_p) = \frac{C_{1A}}{C_{3A}} \times (1-\delta) \times \frac{z_p^{-1}}{1 + (1-\gamma)\left(\frac{C_{2B}}{C_{3A}} - 1\right) z_p^{-1}} \times (V_{IN}(z_p) + V_{REF}(z_p)) \qquad (6.9)$$

where δ and γ are small perturbations proportional to 1/*A*. If the dc gains of the two amplifiers used to implement the path filters in the two-path resonator of Figure 5.3(a) differ, there will be a gain and phase mismatch between the two filter transfer functions. From (5.5) and (5.6), it is apparent that this leads to incomplete suppression of the mirror signal at the output of the two-path resonator. An amplifier dc gain of 1500 (63.5 dB) has been chosen on the basis of behavioral simulations of the two-path modulator that take (6.9) into account. This amount of amplifier gain is sufficient to suppress the mirror signal by at least 40 dB while ensuring that the inband quantization noise power is negligible compared to the estimated thermal noise floor set by the sampling network of the first-stage resonator.

Under linear settling conditions, incomplete amplifier settling only introduces a gain error in the highpass filter transfer function, such that

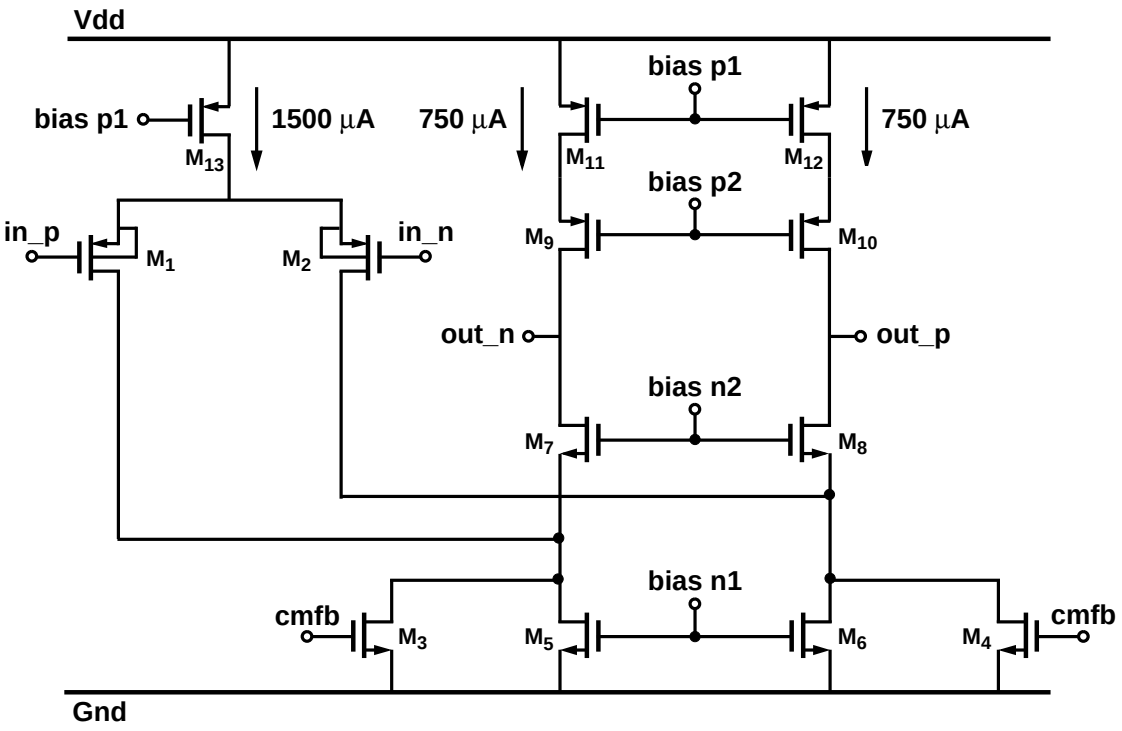
$$V_{OUT}(z_p) = \frac{C_{1A}}{C_{3A}} \times (1-\varepsilon) \times \frac{z_p^{-1}}{1+\left(\frac{C_{2B}}{C_{3A}}-1\right)z_p^{-1}} \times (V_{IN}(z_p) + V_{REF}(z_p)) \qquad (6.10)$$

where $\varepsilon = \exp(-T/\tau)$, T is the time available for settling, and τ is the closed-loop settling time constant. In the two-path resonator of Figure 5.3(a), if the two constituent highpass path filters settle with slightly different time constants, τ_1 and τ_2, then the mirror signal is again incompletely suppressed because the gains of the two path filters are mismatched. Consequently, at least 5τ to 6τ are required for settling so that small variations in τ between the two filters do not cause a substantial gain mismatch. If the amplifier settling has a signal-dependent slewing component, then the effects of incomplete settling upon the two-path resonator cannot be assessed by modeling the highpass path filters with (6.10) [49], [79]. The amplifiers in the first-stage resonator must, in fact, be designed to settle to the full precision of the modulator, which requires a closed-loop settling time of no less than 9τ for a dynamic range of 78 dB. It should be emphasized that distortion due to amplifier slewing can be a concern even at low input signal levels because the full-scale differential reference voltages are fed back to the path filters on every cycle, as indicated by Figure 6.1. In the following chapter, incomplete nonlinear settling is identified as the primary mechanism that limits the performance of the experimental modulator.

6.2 Circuit Design

6.2.1 Folded-Cascode Amplifier

With attention toward the requirements for high bandwidth and a modest dc gain of 1500, the folded-cascode operational amplifier shown in Figure 6.7 was used to implement the switched-capacitor highpass path filters. This topology was chosen over the potentially faster telescopic-cascode topology because its input and output common-mode levels are



Transistor	W/L (μm)	Transistor	W/L (μm)
M1, M2	270/0.6	M9, M10	133.2/0.9
M3, M4	92.4/2.1	M11, M12	482.4/4.8
M5, M6	184.8/2.1	M13	964.8/4.8
M7, M8	66.6/0.9		

Figure 6.7: Folded-cascode operational amplifier.

decoupled from one another and can be set independently. In this design, both the input and output common-mode levels were set to 1.6 V. As seen in Figure 6.8, the simulated unity gain frequency of the amplifier when driving a 2 pF load on each output is approximately 400 MHz with a phase margin of 61°. During the sampling phase, the simulated

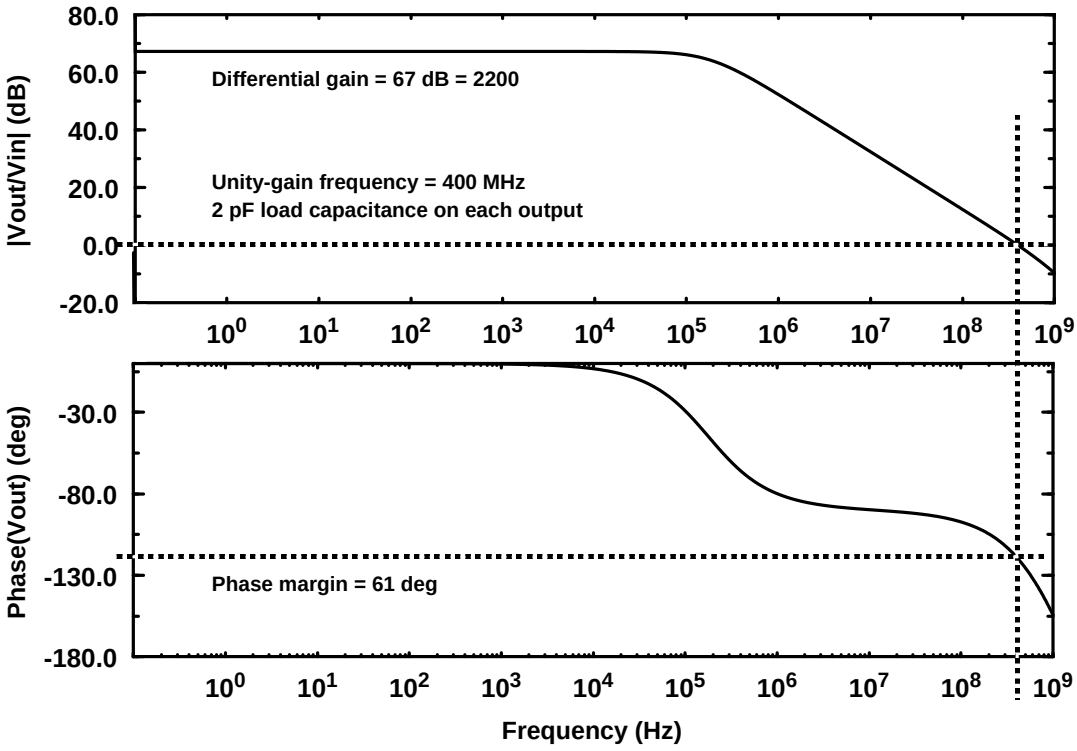


Figure 6.8: Simulated frequency response of the folded-cascode operational amplifier with a 2 pF load capacitance on each output.

closed-loop settling time constant, τ, is approximately 1.5 ns, and during the charge-transfer phase, τ is approximately 2 ns. Thus, when the highpass path filter is clocked at 40 MHz, the settling time is roughly 6τ. The output common-mode level is set by switched-capacitor feedback to the bottom NMOS current source transistors, M_3 and M_4. The common-mode feedback network is shown in Figure 6.9.

Both thermal noise and $1/f$ noise degrade the noise characteristics of the folded-cascode amplifier. However, $1/f$ noise can be neglected in this application because the signal passband is centered at $f_s/4$ while the power of the $1/f$ flicker noise is concentrated around dc. Therefore, considering only thermal noise, the input-referred noise density of the amplifier, $S_{amp}(f)$, is

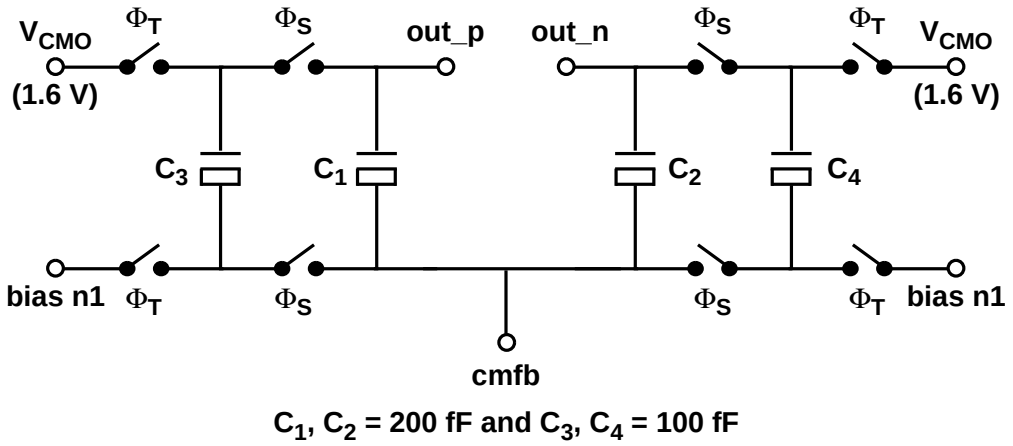


Figure 6.9: Switched-capacitor common-mode feedback.

$$S_{amp}(f) = S_o = 2 \times 4kT \times \gamma \times \frac{1}{g_{m1}} \times \left(1 + \frac{g_{m3} + g_{m5} + g_{m11}}{g_{m1}}\right), \quad 0 < f < \infty. \quad (6.11)$$

In this expression, the initial factor of 2 accounts for the differential topology. For long-channel devices in saturation, the bias-dependent noise factor γ is approximately 2/3. However, recent research indicates that γ can be several times higher for short-channel devices in saturation [99], [100]. Based on measured data, a value of 2 has been assumed for γ in this amplifier [99]. The noise contributions from transistors M_7-M_{10} can be neglected because the noise currents generated in these devices are injected into the output node with a much lower gain than noise currents from transistors M_1-M_2, M_3-M_6, and M_{11}-M_{12}. Noise from current-source transistor M_{13} is neglected because it appears as a common-mode disturbance and is therefore rejected by the fully-differential circuit.

The simulated values of the transconductances in the primary noise-contributing transistors in the folded-cascode amplifier are given in Table 6.1. Based on these values, the estimated value of the input-referred noise amplifier density, $S_{amp}(f)$ can be calculated from (6.11):

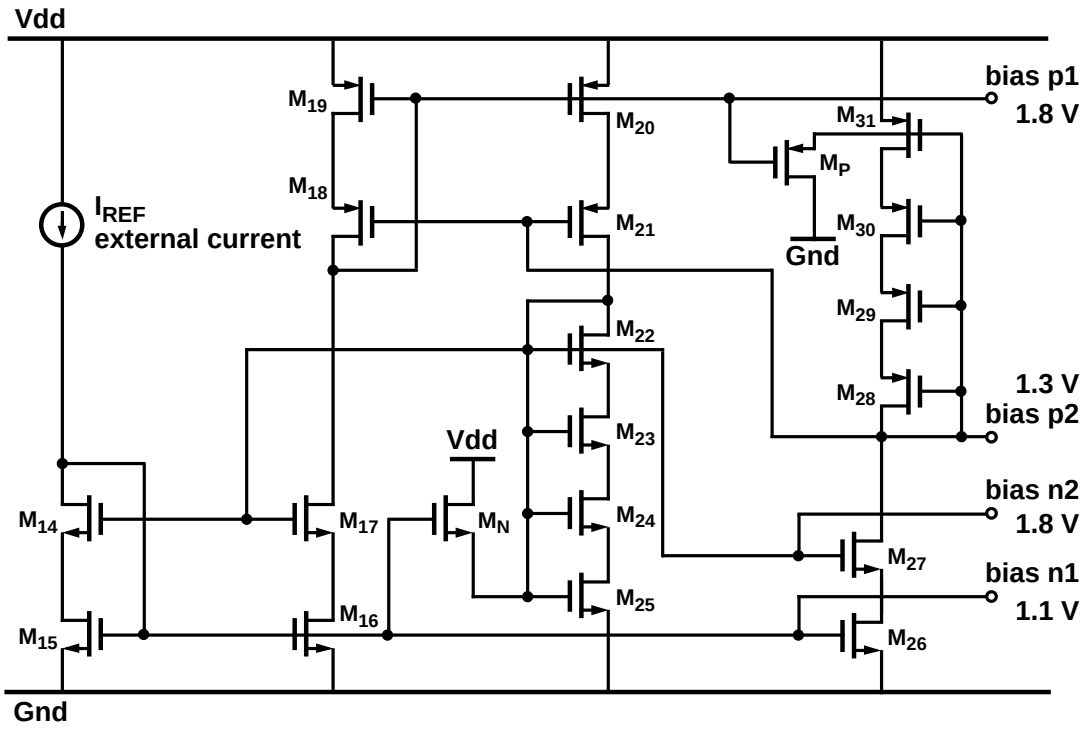
Transistor	g_m (mS)
M1, M2	6.5
M3, M4	2.4
M5, M6	4.9
M11, M12	2.4

Table 6.1: Simulated transconductances of the primary noise-contributing transistors in the folded-cascode amplifier shown in Figure 6.7.

$$\begin{aligned} S_{amp}(f) &= S_o \ , \qquad 0 < f < \infty \\ &= 2 \times 4kT \times \gamma \times \frac{1}{g_{m1}} \times \left(1 + \frac{g_{m3} + g_{m5} + g_{m11}}{g_{m1}}\right) \\ &= 2 \times 4 \times 1.38 \times 10^{-23} JK^{-1} \times 300K \times 2 \times \\ &\quad \frac{1}{6.5mS}\left(1 + \frac{2.4mS + 4.9mS + 2.4mS}{6.5mS}\right) \\ &= 2.54 \times 10^{-17} V^2/Hz \ . \end{aligned} \tag{6.12}$$

6.2.2 Low-Voltage Current Mirrors

Quiescent conditions in the folded-cascode amplifier are established with the biasing circuit shown in Figure 6.10. The transistors in the amplifier are biased such that their drain-source voltage, V_{DS}, is greater than their gate-source overdrive voltage, $V_{GS}-V_T$, by several hundred mV to insure that the transistors remain well within the saturation region of operation, thus maintaining a high output resistance. Low-voltage cascoded current mirrors [101] are used to bias the gates of the NMOS and PMOS current source transistors of the amplifier, M_5-M_6 and M_{11}-M_{13}, to 1.1 V and 1.8 V respectively. The gates of the



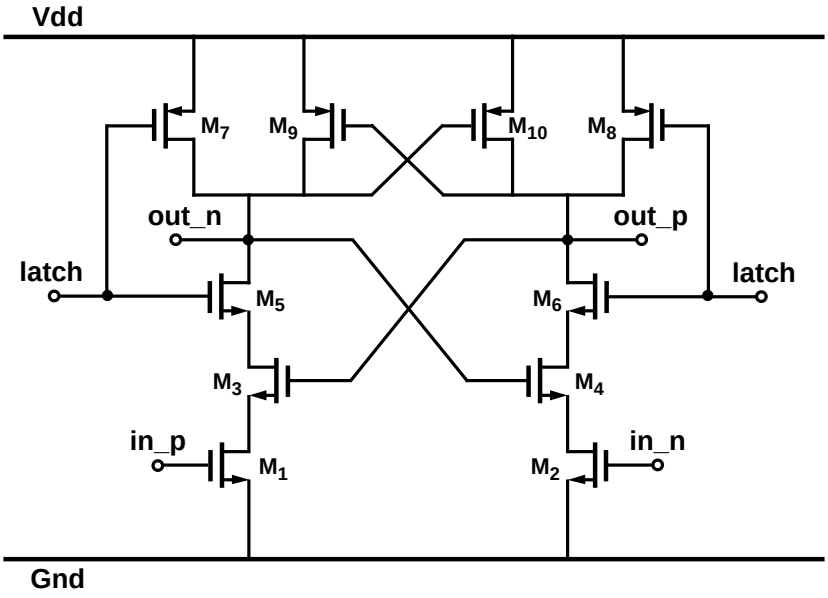
Transistor	W/L (μm)	Transistor	W/L (μm)
M14	22.2/0.9	M24	23.4/2.1
M15	46.2/2.1	M25	17.4/2.1
M16	46.2/2.1	M26	46.2/2.1
M17	22.2/0.9	M27	22.2/0.9
M18	44.4/0.9	M28	44.4/0.9
M19	160.8/4.8	M29	255/4.8
M20	160.8/4.8	M30	177/4.8
M21	44.4/0.9	M31	136.8/4.8
M22	22.2/0.9	MN, MP	2.4/0.6
M23	35.4/2.1		

Figure 6.10: Low-voltage current mirror biasing.

NMOS cascode transistors, M_7 and M_8, are biased with a string of devices, M_{22}-M_{25}, that are operated in the linear region [102]. The NMOS cascode bias voltage, *bias_n*2, is set at a nominal value of 1.8 V. This is a compromise that ensures the NMOS current source transistors, M_3-M_6, are saturated while allowing for a relatively large swing at the amplifier's outputs. Similarly, the gates of the PMOS cascode transistors, M_9 and M_{10}, are biased by a string of devices in their linear region, M_{28}-M_{31}, to a nominal voltage of 1.3 V. Small transistors, M_N and M_P, insure that the bias circuit settles to the desired operating point instead of a stable, zero-current state. All transistors in Figure 6.10, with the exception of M_N and M_P, have nonminimum channel lengths in order to reduce the influence of channel length modulation on the bias voltages. The operating conditions in the bias circuit are established with an external reference current, I_{REF}, that is applied to M_{14} and M_{15} and mirrored in the different branches of the circuit. In order to reduce layout complexity, but at the expense of increased power dissipation, the experimental modulator contains four independent biasing circuits, one for each operational amplifier.

6.2.3 Comparator

The two 1-b quantizers in Figure 5.9 are realized using a fast dynamic latch [103] followed by buffers and a set-reset (SR) latch that holds the data for a full clock cycle. The dynamic latch is shown in Figure 6.11. Preamplification is not required because each path of the proposed modulator is relatively insensitive to errors introduced at the inputs to the respective quantizers. However, as discussed in Section 5.3.1, gross mismatch of offset and hysteresis between the two quantizers can generate tones in the output spectrum at dc and $f_s/2$, as well as adversely affect the degree of mirror signal suppression that is achieved at the output of the modulator. In the interest of reducing the input-referred offsets of each quantizer, nonminimum channel length transistors are used in the regenerative cores of both comparators.



Transistor	W/L (μm)	Transistor	W/L (μm)
M1, M2	9/1.5	M7, M8	12/1.5
M3, M4	9/1.5	M9, M10	24/1.5
M5, M6	4.5/1.5		

Figure 6.11: Dynamic latch used as the comparator core.

6.2.4 Two-Phase Clock Generator

The clock phases for the modulator are generated using a fully-differential, two-phase clock generator [104] that is driven by a reference clock, Φ_R and $\overline{\Phi_R}$, supplied from an external source. A block diagram of the two-phase clock generator is shown in Figure 6.12, and the fully-differential logic gates used in its implementation are illustrated in Figures 6.13(a) and (b). Buffers comprised of inverters are used to distribute the various

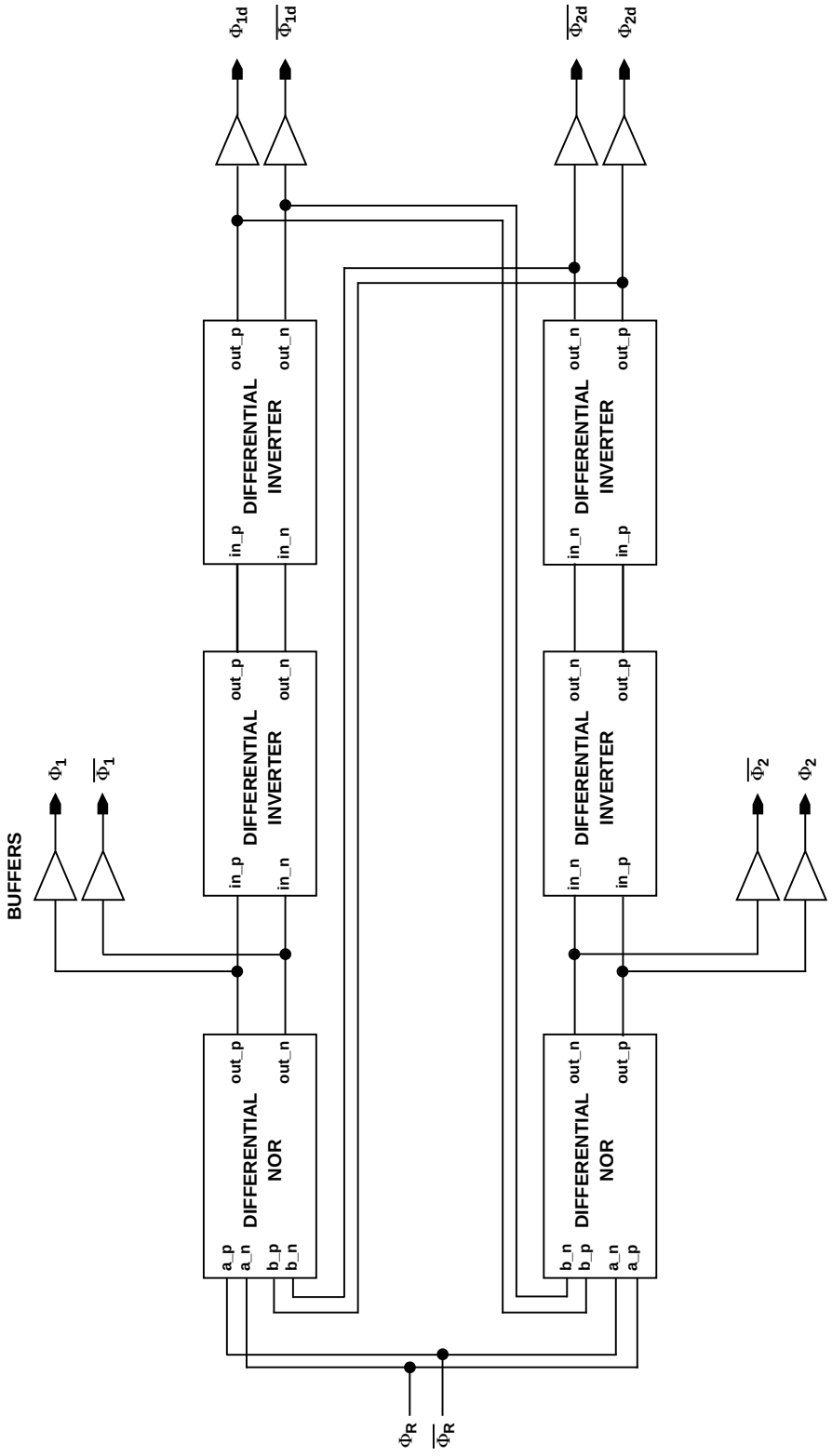
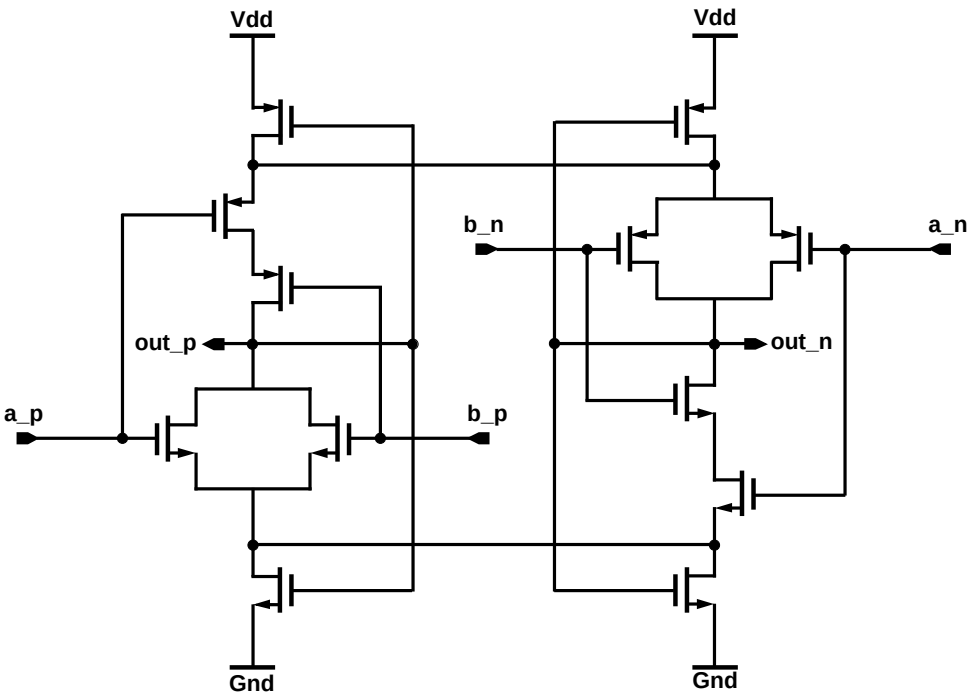
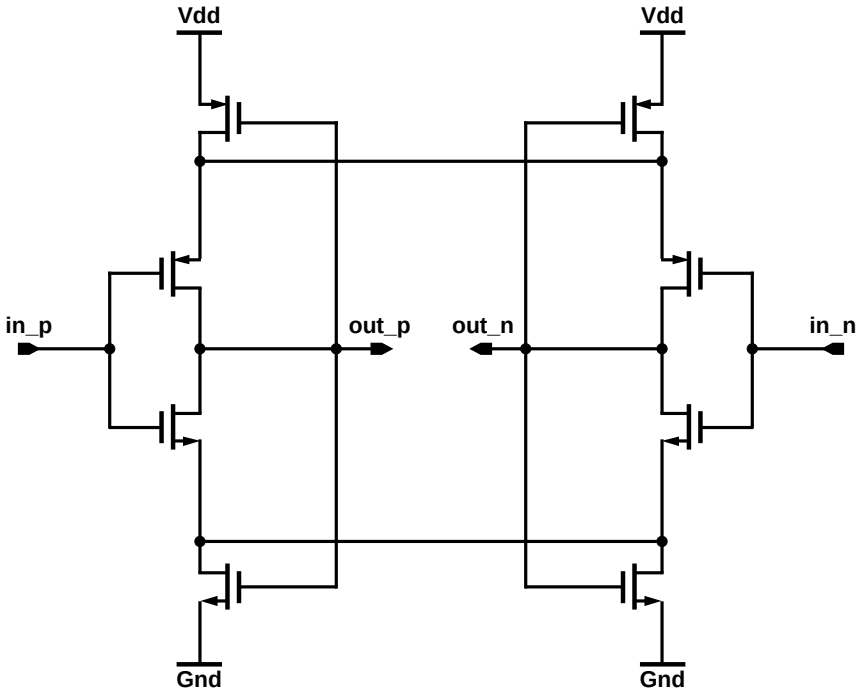


Figure 6.12: Two-phase clock generator.



(a)



(b)

Figure 6.13: Differential logic gates, (a) NOR and (b) inverter.

clock phases throughout the chip. The use of a fully-differential clock topology is especially convenient in this application because the complements of the clocks are generated automatically, without the use of any additional inverters. Therefore, the potential for introducing skew between clocks and their complements is avoided.

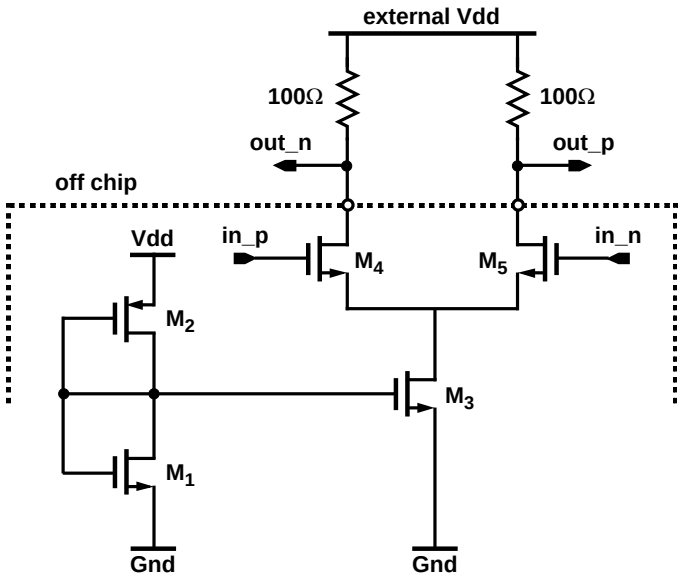
6.2.5 Output Drivers

The outputs from the comparators are brought off chip as fully-differential, current-mode signals using the driver shown in Figure 6.14. The open drains of the differential pair comprised of M_4 and M_5 are connected to 100 Ω pullup resistors on the test board, which are tied to an external 3.3 V power supply that is not shared with the integrated circuit. The tail current source, M_3, is biased to approximately 1 mA by diode-connected transistors M_1 and M_2.

The use of current-mode outputs with small pullup resistors ensures that the voltage swings across the bond wires is small, thus reducing the amount of noise coupling through mutual inductance to adjacent sensitive nodes. Also, since the voltage swing at the output pads is small, the amount of noise injected into the substrate through the large parasitic capacitance that exists between the pad and substrate is minimized.

6.3 Noise Analysis of the Proposed Two-Path Modulator

Section 6.1.3 and Section 6.1.4 discussed the effects of switch and amplifier noise on the performance of the switched-capacitor highpass path filter depicted in Figure 6.1. The following section extends this discussion to the entire two-path modulator. The total inband noise power of the two-path modulator is estimated assuming that quantization noise is negligible with respect to switch and amplifier noise in the circuit.



Transistor	W/L (μm)	Transistor	W/L (μm)
M1	26.4/1.2	M3	151.2/0.6
M2	6/1.2	M4, M5	60/0.6

Figure 6.14: Current-mode output driver.

6.3.1 Switch Noise

Thermal noise from the switches can be referred to the inputs of each switched-capacitor filter as discussed in Section 6.1.3, and then referred to the input of the two-path modulator. However, the calculation can be simplified by neglecting switch noise from the second-stage filter because it is attenuated by noiseshaping. The total power of the switch noise referred to the input of the first-stage filter was calculated in Section 6.1.3 as:

$$\overline{e^2_{switch}} = kT\left(\frac{2}{C_{1A}} + \frac{2}{C_{1B}} + \frac{2}{C_{2A}} + \frac{2}{C_{2B}}\right) \tag{6.13}$$

$$= 1.38\times10^{-23}JK^{-1}\cdot 300K\cdot\left(\frac{2}{300\,fF} + \frac{2}{300\,fF} + \frac{2}{1.5\,pF} + \frac{2}{1.5\,pF}\right)$$

$$= 6.624\times10^{-8}V^2\,.$$

Since the input of the first-stage filter constitutes the front-end of the two-path modulator, the total switch noise referred to the modulator's input is also given by (6.13). It is assumed that the switch bandwidth is much larger than the sampling frequency in the modulator, so $\overline{e^2_{switch}}$ is uniformly distributed throughout the sampling bandwidth. Because the passband bandwidth is only a fraction of the sampling bandwidth, the contribution to the inband noise power is equal to (6.13) divided by the oversampling ratio, *M*. For $M=200$, this leads to

$$\overline{e^2_{switch,\,inband}} = \frac{kT}{M}\left(\frac{2}{C_{1A}} + \frac{2}{C_{1B}} + \frac{2}{C_{2A}} + \frac{2}{C_{2B}}\right) \tag{6.14}$$

$$= 6.624\times10^{-8}V^2/200 = 3.312\times10^{-10}V^2\,.$$

Although, the front-end of the modulator is comprised of two highpass filters, one in the Φ_1 path and the other in the Φ_2 path, the input-referred switch noise power is not doubled because the modulator outputs are interleaved rather than summed.

If the input-referred noise of the proposed two-path modulator is dominated by *kT*/*C* noise in the two first-stage highpass filters, then the dynamic range of the modulator is

$$DR = \frac{\frac{1}{2}\left(\frac{\Delta}{2}\right)^2}{\overline{e^2_{switch,\,inband}}}\,. \tag{6.15}$$

In the experimental prototype, Δ is equal to 1.0 V, so the estimated dynamic range of the modulator is 86 dB if switch noise is the dominant thermal noise source in the circuit. However, as the experimental results presented in Chapter 7 indicate, the noise in the sig-

nal bandwidth is approximately –77 dB, where the 0 dB level is defined as the power of a sinusoid with amplitude Δ/2. This loss in the dynamic range of the modulator can be attributed to electronic noise from the operational amplifiers and is quantified in the following two sections, 6.3.2 and 6.3.3.

6.3.2 Operational Amplifier Noise

The effect of amplifier noise in the proposed two-path modulator is assessed by analyzing a single highpass path of the modulator with two independent amplifier noise sources, e_{amp1} and e_{amp2}. A block diagram of the noisy highpass modulator is shown in Figure 6.15. Once again, a single-ended representation is used for simplicity, and it is recognized that the –1 buffers represent the interchange of terminals in the fully-differential circuit.

If the quantizer in Figure 6.15(b) is modeled as a gain, G_Q, with an additive noise source, E(z), it can be shown that the output of the highpass modulator is described in the z-domain by

$$Y(z_p) = \frac{-0.2G_Q \cdot z_p^{-2} X(z_p) + (1 + z_p^{-1})^2 E(z_p)}{1 + (2 - 0.5G_Q) \cdot z_p^{-1} + (1 - 0.3G_Q) \cdot z_p^{-2}} + NTF_{amp1}(z_p) e_{amp1}(z_p) + NTF_{amp2}(z_p) e_{amp2}(z_p) \tag{6.16}$$

where the noise transfer functions for e_{amp1} and e_{amp2} are respectively,

$$NTF_{amp1}(z_p) = \frac{-0.5G_Q \cdot z_p^{-1}(1 + 2.4z_p^{-1/2} - z_p^{-1})}{1 + (2 - 0.5G_Q) \cdot z_p^{-1} + (1 - 0.3G_Q) \cdot z_p^{-2}} \tag{6.17}$$

and

$$NTF_{amp2}(z_p) = \frac{0.5G_Q \cdot (1 + z_p^{-1}) \cdot (2 + 5z_p^{-1/2} - 2z_p^{-1})}{1 + (2 - 0.5G_Q) \cdot z_p^{-1} + (1 - 0.3G_Q) \cdot z_p^{-2}} . \tag{6.18}$$

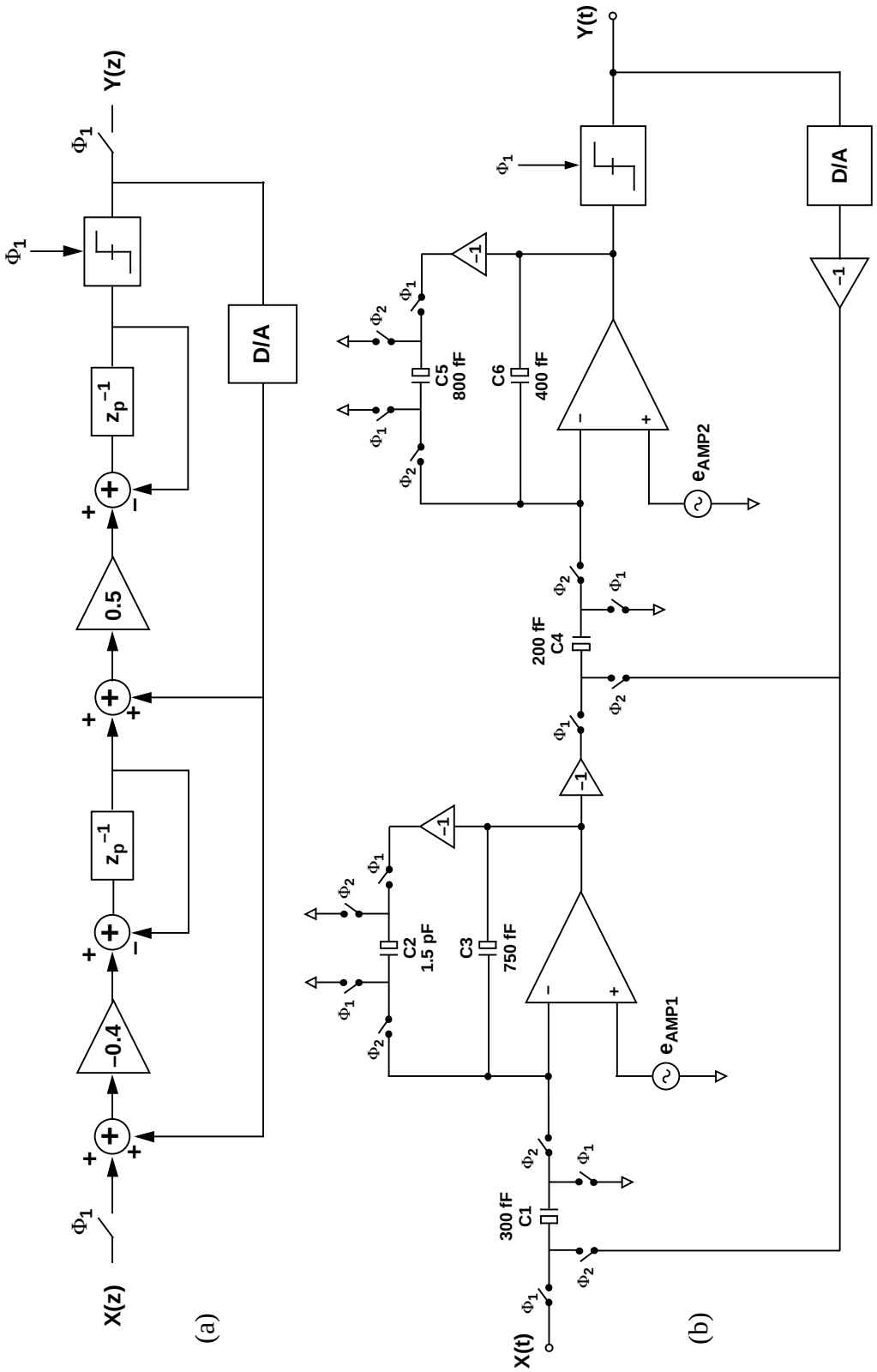


Figure 6.15: (a) Block diagram and (b) single-ended switched-capacitor realization of a single path of the proposed two-path modulator with amplifier noise modeled by two independent sources, e_{amp1} and e_{amp2}.

Recall that z_p^{-1} is interpreted as a single delay with respect to the sampling rate of a single path. Equations (6.16), (6.17), and (6.18) can be simplified by setting the gain of the quantizer, G_Q, to 5 as was done in Section 4.1.2. This yields

$$NTF_{amp1}(z_p) = \frac{-2.5z_p^{-1}(1 + 2.4z_p^{-1/2} - z_p^{-1})}{1 - 0.5z_p^{-1} - 0.5z_p^{-2}} \tag{6.19}$$

and

$$NTF_{amp2}(z_p) = \frac{2.5(1 + z_p^{-1})(2 + 5z_p^{-1/2} - 2z_p^{-1})}{1 - 0.5z_p^{-1} - 0.5z_p^{-2}} , \tag{6.20}$$

which, in the frequency domain, can be written as

$$\begin{aligned} NTF_{amp1}(f) &= NTF_{amp1}(z_p)\Big|_{z_p = e^{j2\pi f T_{ps}}} = \\ &= \frac{-2.5e^{-j2\pi f T_{ps}}(1 + 2.4e^{-j2\pi f T_{ps}/2} - e^{-j2\pi f T_{ps}})}{1 - 0.5e^{-j2\pi f T_{ps}} - 0.5e^{-j4\pi f T_{ps}}} \end{aligned} \tag{6.21}$$

and

$$\begin{aligned} NTF_{amp2}(f) &= NTF_{amp2}(z_p)\Big|_{z_p = e^{j2\pi f T_{ps}}} = \\ &= \frac{2.5(1 + e^{-j2\pi f T_{ps}})(2 + 5e^{-j2\pi f T_{ps}/2} - 2e^{-j2\pi f T_{ps}})}{1 - 0.5e^{-j2\pi f T_{ps}} - 0.5e^{-j4\pi f T_{ps}}} \end{aligned} \tag{6.22}$$

where T_{ps} is the path sampling period. If $\overline{e_{amp1}^2}$ is the input-referred noise power of the first-stage amplifier, then the spectral density of the shaped noise from e_{amp1} is

$$S_{amp1,\,out}(f) = \left|NTF_{amp1}(f)\right|^2 \times \frac{\overline{e_{amp1}^2}}{f_{ps}} , \qquad -\frac{f_{ps}}{2} < f < \frac{f_{ps}}{2} . \tag{6.23}$$

Similarly, the spectral density of the shaped noise from e_{amp2} is

$$S_{amp2,\,out}(f) = \left|NTF_{amp2}(f)\right|^2 \times \frac{\overline{e_{amp2}^2}}{f_{ps}} \ , \qquad -\frac{f_{ps}}{2} < f < \frac{f_{ps}}{2} \tag{6.24}$$

given that $\overline{e_{amp2}^2}$ is the input-referred noise power of the second-stage amplifier.

Next, it is noted that the signal passband is centered at $\pm f_{ps}/2$, and the passband bandwidth is assumed to be much less than f_{ps}. Therefore, in the passband, the spectral density of the shaped noise from e_{amp1} and e_{amp2} can be approximated as

$$\begin{aligned} S_{amp1,\,inband}(f) &\approx S_{amp1,\,out}(f)\big|_{f\,=\,f_{ps}/2} \\ &= \left|NTF_{amp1}(f)\big|_{f\,=\,f_{ps}/2}\right|^2 \times \frac{\overline{e_{amp1}^2}}{f_{ps}} \\ &= 61 \times \frac{\overline{e_{amp1}^2}}{f_{ps}} \end{aligned} \tag{6.25}$$

and

$$\begin{aligned} S_{amp2,\,inband}(f) &\approx S_{amp2,\,out}(f)\big|_{f\,=\,f_{ps}/2} \\ &= \left|NTF_{amp2}(f)\big|_{f\,=\,f_{ps}/2}\right|^2 \times \frac{\overline{e_{amp2}^2}}{f_{ps}} \\ &= 0 \times \frac{\overline{e_{amp2}^2}}{f_{ps}} = 0 \ . \end{aligned} \tag{6.26}$$

The important and disturbing implication of (6.25) is that within the passband, noise power from the first-stage amplifier is amplified by a factor of 61 at the output of the filter. Fortunately, (6.26) indicates that the inband noise contribution from the second-stage amplifier is negligible because the noise shaping function $NTF_{amp2}(f)$ has a zero at $f_{ps}/2$. From (6.25) and (6.26), the power of the amplifier noise present in the signal band is approximately

$$\overline{e^2_{amp,\,inband}} \approx [S_{amp1,\,inband}(f) + S_{amp2,\,inband}(f)] \times B \tag{6.27}$$

$$\approx 61 \times \frac{\overline{e^2_{amp1}}}{f_{ps}} \times B$$

where B is the width of the passband.

The value of $\overline{e^2_{amp,\,inband}}$ for the prototype modulator can be estimated from (6.27) once $\overline{e^2_{amp1}}$ has been calculated. From (6.7),

$$\overline{e^2_{amp}} = S_o \times \frac{1}{2\pi\tau_{cl}} \times \frac{\pi}{2} \tag{6.28}$$

where S_o is the input-referred amplifier white noise density, and τ_{cl} is the closed-loop settling time constant of the highpass path filter. In Section 6.2.1, it is estimated that $S_o = 2.54{\times}10^{-17}$ V^2/Hz and $\tau_{cl} = 1.5$ ns for the folded-cascode amplifier used in the prototype modulator. Therefore, by (6.28), this amplifier's input-referred noise power, $\overline{e^2_{amp1}}$, is approximately $4.23{\times}10^{-9}$ V^2. Given a path sampling frequency, f_{ps}, of 40 MHz, and passband bandwidth, B, of 200 kHz, the estimated contribution to the total output noise power from e_{amp1} and e_{amp2} is

$$\overline{e^2_{amp,\,inband}} \approx 61 \times \frac{\overline{e^2_{amp1}}}{f_{ps}} \times B \tag{6.29}$$

$$= 61 \times \frac{4.23 \times 10^{-9} V^2}{40 MHz} \times 200 kHz$$

$$= 1.29 \times 10^{-9} V^2 \ .$$

Once again, although the experimental prototype is comprised of two interleaved highpass modulators, the output-referred amplifier noise of the entire two-path modulator is not twice the value calculated in (6.29) because the outputs are interleaved, not summed. In comparison with (6.14), it can be seen that inband noise contributed by the first-stage amplifier is several times larger than the inband kT/C noise.

6.3.3 Calculated Front-End Noise

If it is assumed that quantization noise is negligible with respect to switch and amplifier noise, the estimated dynamic range of the two-path modulator with $\Delta = 1.0$ V is

$$DR = \frac{\frac{1}{2}\left(\frac{\Delta}{2}\right)^2}{\overline{e^2_{switch,\,inband}} + \overline{e^2_{amp,\,inband}}} \tag{6.30}$$

$$= \frac{\frac{1}{2}\left(\frac{1.0V}{2}\right)^2}{3.312 \times 10^{-10}V^2 + 1.29 \times 10^{-9}V^2}$$

$$= 7.71 \times 10^7 = 79 \;\; dB \;\; .$$

This estimate is confirmed by the experimental results presented in Chapter 7; the measured inband noise power of the prototype modulator is approximately 77 dB below overload (0 dB), which is defined as the power of a sinusoid with amplitude $\Delta/2$.

6.4 Summary

The implementation of the proposed two-path, $f_s/4$ modulator has been described in this chapter. A fully-differential, switched-capacitor path filter that implements the desired highpass transfer function has been designed, and its limitations due to switch and amplifier noise, as well as finite amplifier gain and bandwidth, have been analyzed. Although the use of the two-path modulator topology relaxes the settling requirements on the operational amplifiers, behavioral simulations indicate that the amplifiers must still have at least 5 to 6 time constants to settle because small mismatches in the settling times between the two paths will degrade the suppression of the mirror signal. A folded-cascode amplifier with a closed-loop, simulated settling time constant of approximately 2 ns was designed to meet these requirements when the path filter is clocked at 40 MHz. The amplifier is biased by low-voltage current mirrors that are programmed by an external current.

Additional circuits in the prototype described in this chapter include the dynamic comparators, a two-phase clock generator, and the output drivers. The comparators are simple regenerative cores followed by buffers and SR latches. The two-phase clock generator is implemented using fully-differential logic gates so that the necessary clock phases and their complements can be generated without introducing unnecessary skew between the clocks and their complements. The output drivers bring the one-bit data streams from each path off chip as fully-differential current-mode signals to reduce the amount of noise coupling through bond wire mutual inductance, substrate injection, and power supply disturbance.

A noise analysis of the entire two-path modulator reveals that the noise floor of the experimental prototype is dominated by a combination of amplifier noise and thermal noise from the switches. As a strong caveat, it is noted that amplifier noise in the first-stage path filter is shaped to have a maximum spectral density in the signal band centered at $f_s/4$. This hazardous noise amplification can degrade the dynamic range of the modulator by a substantial margin if some care is not taken to design an operational amplifier with a low enough input-referred noise power such that at the output of the modulator, the level of shaped amplifier noise in the passband remains comparable to the level of inband kT/C noise.

Chapter 7 *Experimental Results*

An experimental prototype of the proposed two-path, $f_s/4$ modulator described in the preceding chapters has been fabricated in a 0.6-μm, single-poly, triple-metal CMOS process through the MOSIS service. When operated from a 3.3-V supply, the experimental modulator dissipates 49 mW, and the clock generator dissipates an additional 23 mW. An estimated 40% of the power dissipated in the analog circuitry is devoted to driving the large bottom-plate parasitics of the feedback and sampling capacitances. Thus, the power dissipation could be reduced significantly in a technology with a smaller bottom-plate parasitic. Also, the currents and device sizes in the second stage of the modulator could be scaled more aggressively. In this prototype, to expedite the design, the first and second stages of the modulator were implemented using identical operational amplifiers. Only capacitances were scaled in the second stage.

This chapter describes the layout of the prototype chip, the test setup used to characterize the experimental circuit, and the measured results.

7.1 Layout

A die photo of the experimental prototype is shown in Figure 7.1. Mirror symmetry was observed in the layout to enhance the rejection of common-mode disturbances in the fully-differential circuit. The front-end, differential inputs to the modulator are at the far left of the die. The digital circuits, seen at the right of Figure 7.1, are physically separated from the analog circuits and are powered from a separate supply. The use of different analog and digital supplies decouples the analog circuitry from the switching noise caused by large dynamic currents drawn from the digital supply.

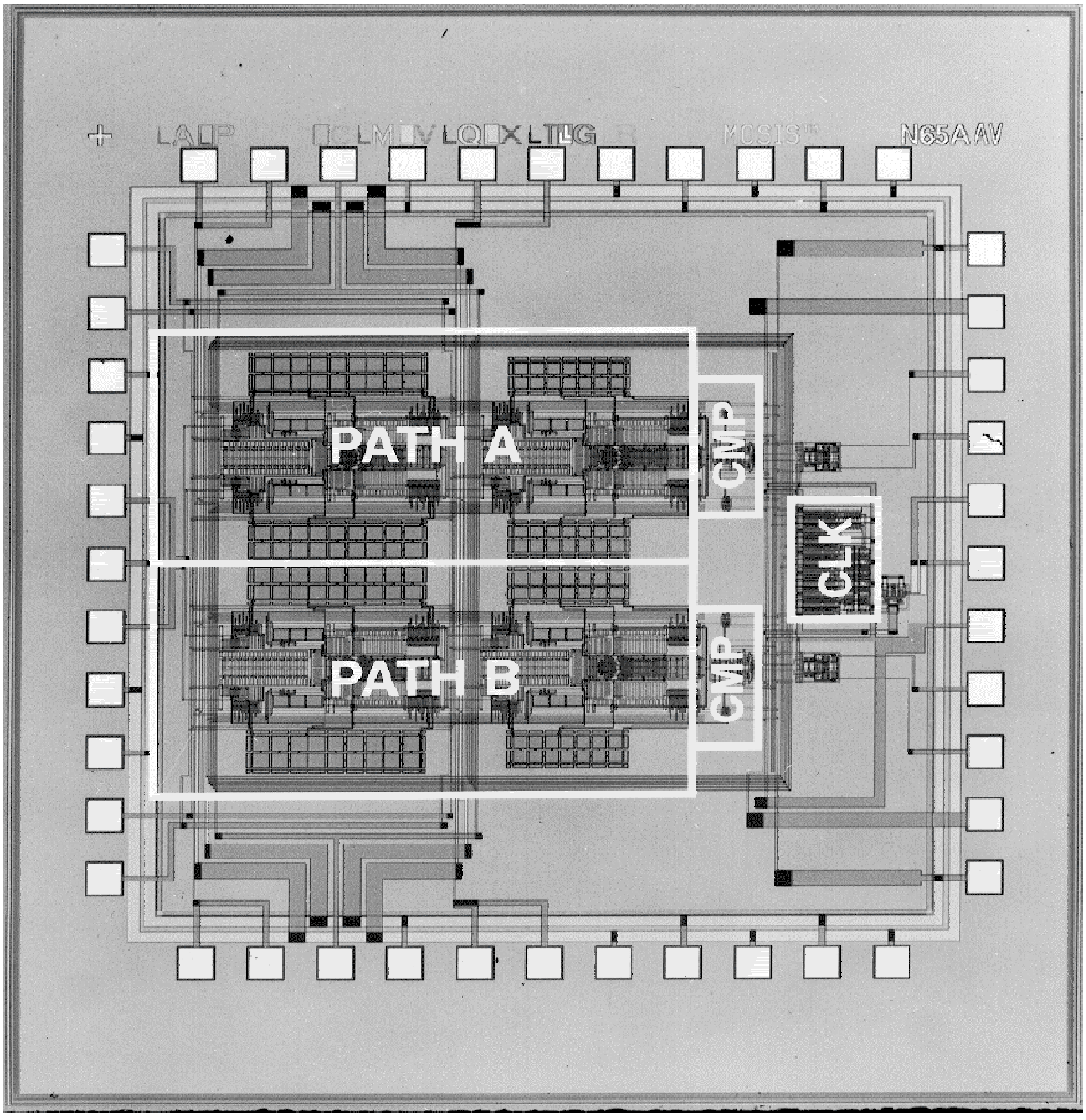


Figure 7.1: Die photo of the prototype two-path modulator.

Within the chip, the digital ground is also separate from the analog ground in order to reduce the amount of digital switching noise that is coupled into the substrate [105], [106]. Since the substrate contacts are tied to analog ground, disturbances on the digital ground induced by dynamic currents are not directly manifested in the substrate. The penalty incurred by separating the substrate contacts from the digital ground lines is that the area of the digital circuitry is increased slightly. In this prototype, the digital circuitry occupies a relatively small portion of the total area, so the increase is negligible. The active area of the prototype chip measures only $1.3\text{ mm} \times 2.1\text{ mm}$. However, in a large and predominantly digital ASIC, of which only a small fraction of the chip area is likely to be devoted to a precision mixed-signal circuit such as this bandpass A/D converter, it may not be feasible to wire the digital ground separately from the substrate contacts. Instead, the substrate contacts are wired directly to the local supplies, which unfortunately results in the highest degree of noise injection into the substrate. Nevertheless, in such cases, a first-order insensitivity to substrate effects and other common-mode disturbances can still be derived by utilizing fully-differential circuits with a symmetric layout.

As discussed in Section 6.1.5, the stability of the modulator is affected by the degree of mismatch between capacitors in the highpass path filters. Capacitor mismatch can cause the pole of the filter to lie outside of the unit circle. Therefore, in keeping with standard practice, the capacitances were formed by connecting unit cells arranged in an array [107], [108]. A layout example is shown in Figure 7.2. The unit cell has a nominal capacitance of 150 fF; the 300 fF, 750 fF, and 1.5 pF necessary for the first stage of the modulator are formed by interconnecting two, five, and ten unit cells respectively. Because the necessary capacitors are integer multiples of the unit cell, the area-to-perimeter ratio is kept constant among the different capacitors. For example, it is seen in Figure 7.2 that the area and perimeter of the 750 fF capacitor are both 2.5× that of the 300 fF capacitor, thus ensuring that the contributions to the total capacitance from plate-to-plate fields as well as fringing effects are both multiplied by 2.5×. Dummy capacitors placed along the outside edge of the capacitor array guarantee that the fringing fields at the periphery of the array are iden-

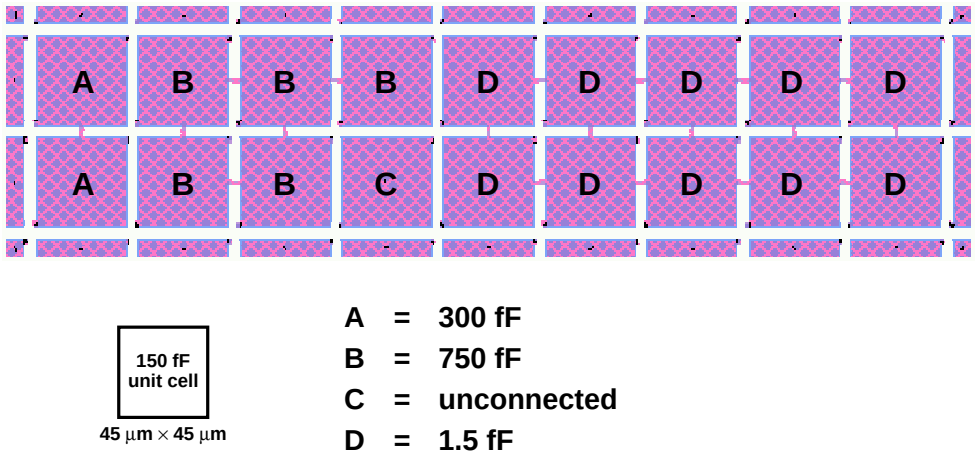


Figure 7.2: An example layout of matched 300 fF, 750 fF, and 1.5 pF capacitors using a 150 fF unit cell and dummy strips lining the periphery of the array.

tical to those in the interior and insure that the unit cells are etched uniformly along all sides.

7.2 Test Setup

A diagram of the experimental test setup is shown in Figure 7.3. The test board is a two-sided, copper-clad board with separate analog and digital ground planes that are connected together at the power supplies. The device under test (DUT) was packaged in a 44-pin, J-lead, ceramic quad flat pack and placed in a surface-mount PLCC socket on the test board. The supply pins were bypassed with 0.01-μF chip capacitors at the leads of the socket.

A separate board was used to generate all of the regulated voltages and currents that power the device under test and serve as references to the chip. A full description of these circuits is given in [104], [109]. Within the chip, the digital circuitry is powered by a separate supply, denoted *DVdd*. In addition, the analog and digital circuits on the test board are powered from supplies separate from those used to power the device under test. The outputs from the two paths in the modulator are brought off chip as fully-differential, cur-

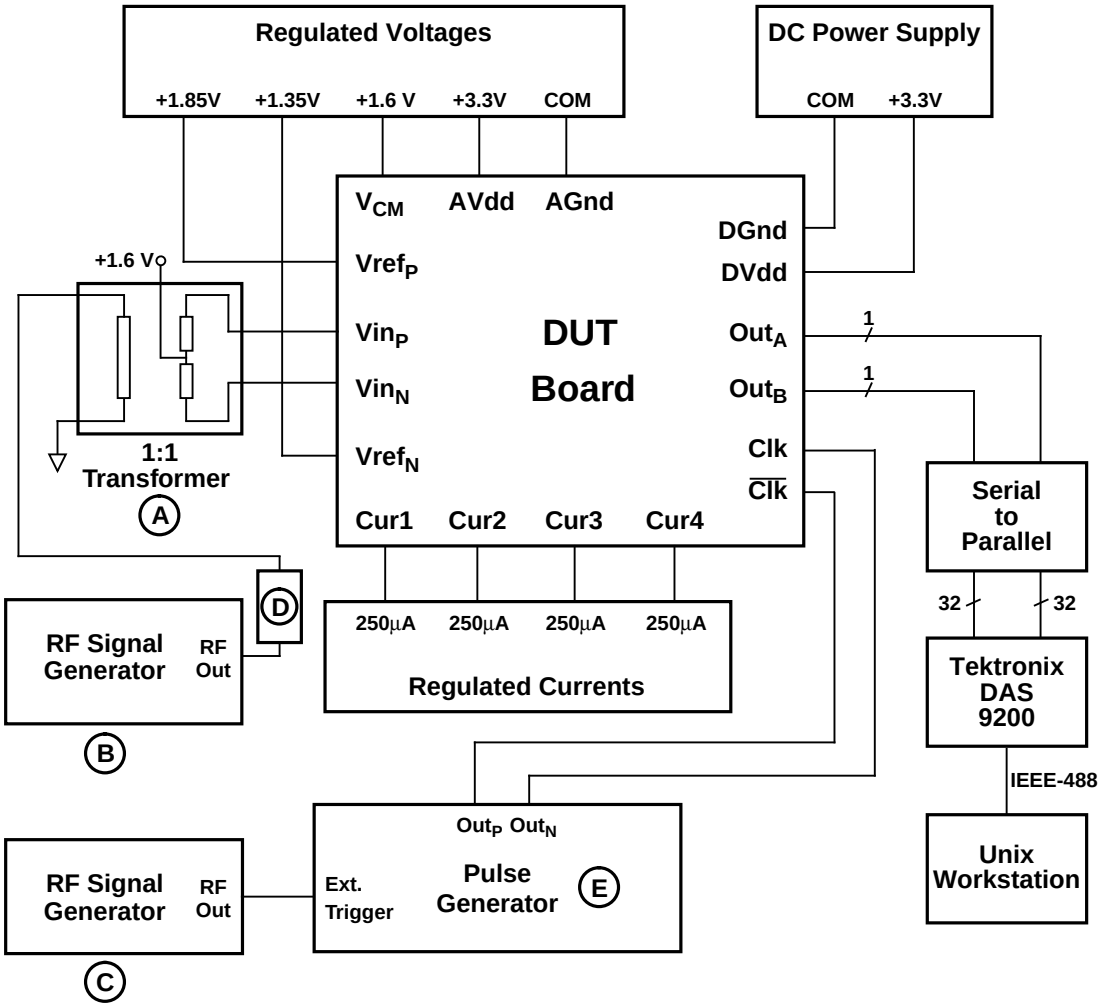


Figure 7.3: Experimental test setup.

rent-mode signals, which are tied to pullup resistors on the test board as described in Section 6.2.5. The resulting low-swing voltage signals are amplified to full CMOS logic levels by fast AD9696 comparators before being harvested by a custom serial-to-parallel interface board.

The differential input to the modulator was generated by driving an external, center-tapped transformer with the filtered output of a low phase noise, single-ended sinusoidal source locked to various test frequencies near 20 MHz. The filter at the output of the RF generator suppresses the higher-order harmonics of the input signal before they are passed to the device under test. The differential sinusoid is applied directly to the inputs of the modulator. The reference voltages of the modulator were tied to V_{REF+} = 1.85 V and V_{REF-} = 1.35 V. In the subsequent plots of performance as a function of the signal level, 0 dB corresponds to the power of a differential sine wave input of 1.0 $V_{p\text{-}p}$.

A low-swing, differential clock from an external pulse generator triggered by a low phase-noise signal source locked at 40 MHz was brought on chip, amplified to full swing, and then used to generate the requisite clock phases. The custom interface board collects 640,000 samples from each of the two independent paths of the modulator, *A* and *B,* and then transfers this data to a workstation for interleaving, filtering, and analysis. Figure 7.4 shows an FFT of the interleaved bitstream, prior to decimation, when a –10 dB input signal is applied to the modulator.

The degree of mirror signal suppression in the modulator was evaluated by demodulating the bandpass signal to baseband with quadrature carriers in the digital domain and performing an FFT on the resulting complex-valued signal, $x_I[n] - jx_Q[n]$. The spectrum of the demodulated, complex-valued baseband signal is shown in Figure 7.5. It is seen that the mirror signal is suppressed by 42 dB with respect to the desired signal.

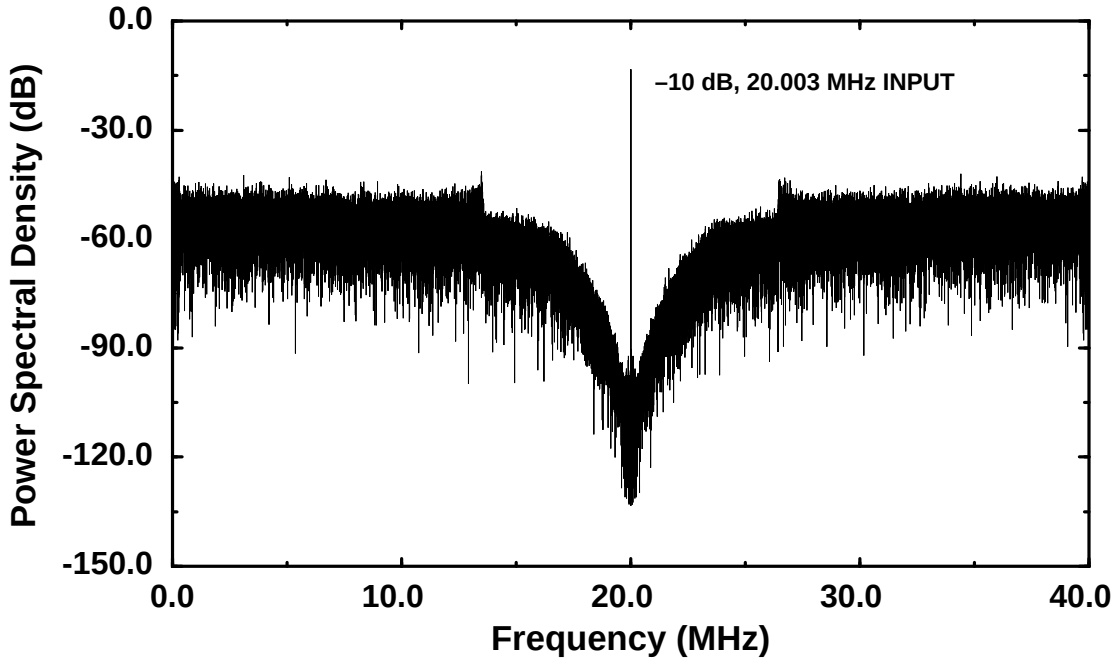


Figure 7.4: Spectrum of undecimated bitstream.

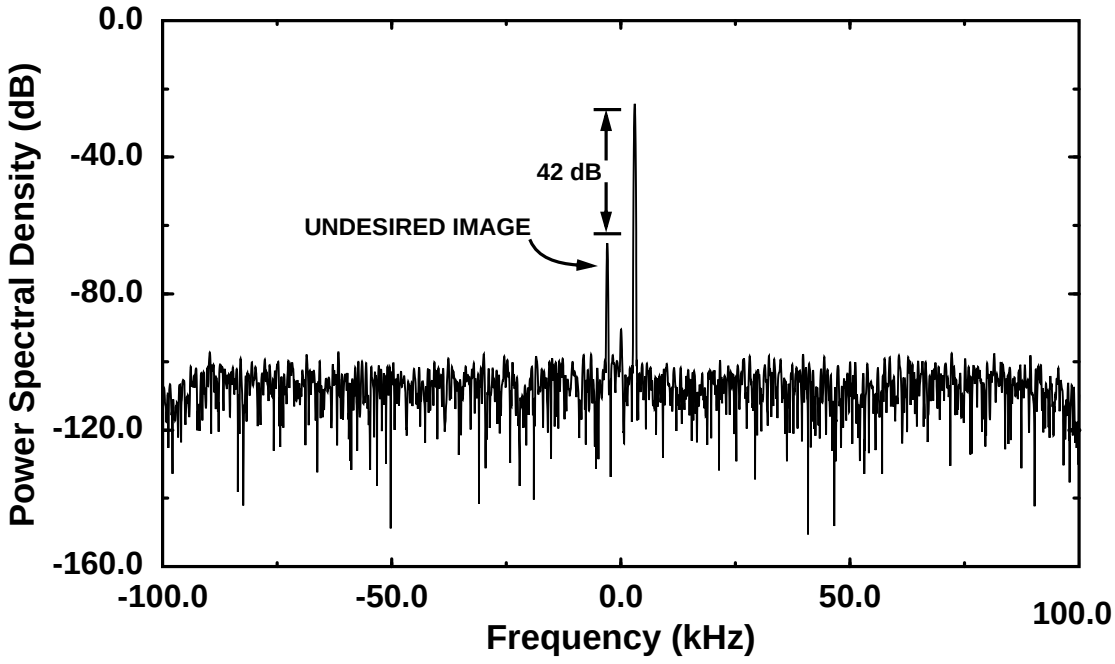


Figure 7.5: Spectrum of complex baseband signal.

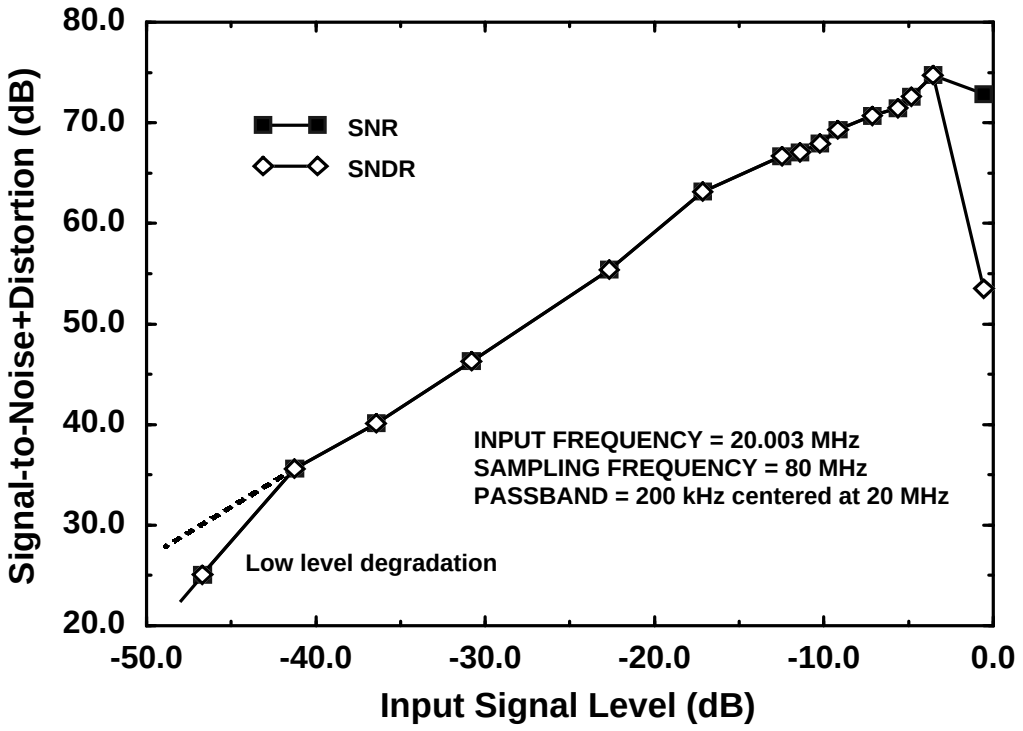


Figure 7.6: Measured SNR and SNDR.

7.3 Measured Performance

7.3.1 SNR and SNDR

The plots of the SNR and SNDR versus input signal level shown in Figure 7.6. indicate that the experimental prototype achieves a peak signal-to-noise ratio (SNR) of 72 dB in a passband of 200 kHz centered at 20 MHz. However, the noise floor increases as the input signal level drops below approximately –40 dB. This degradation is most likely the result of mixing between the input signal and tones in the noise spectrum.

As the input signal level drops below approximately –40 dB, large families of tones appear at dc and $f_s/2$, where f_s is the effective sampling frequency of the modulator, 80 MHz. These tones, seen in the undecimated output spectrum of Figure 7.7, defy explicit analytical representation, but their influence can be qualitatively assessed. First, it

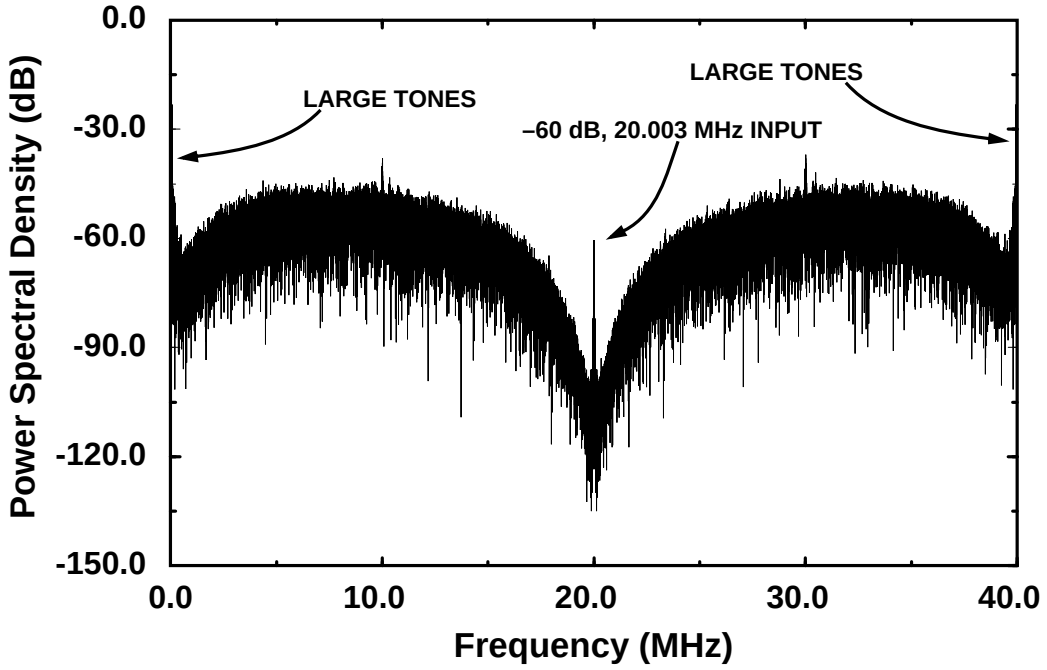


Figure 7.7: Tones in the undecimated spectrum.

should be emphasized that high-level tones at dc and $f_s/2$ are not unique to the two-path architecture. Rather, they are present in many classes of bandpass, as well as lowpass [52], [53] modulators, and they are readily observed in behavioral simulations. As discussed in Chapter 3, the existence of tones at dc and $f_s/2$ are especially significant in bandpass modulators that center the signal passband at $f_s/4$ because, through nonlinear mechanisms, the tones can mix with the input signal and fall into the passband.

At an 80 MHz sampling frequency, as the input signal level decreases, increased harmonic distortion and a higher noise floor are observed in the experimental prototype. However, if the sampling frequency is reduced to 40 MHz, the harmonic distortion disappears and the noise floor remains essentially constant for all input signal levels. The fact that the degradation is more pronounced at high sampling speeds suggests that nonlinear operational amplifier settling is the root cause of mixing between the signal and the tones at dc and $f_s/2$.

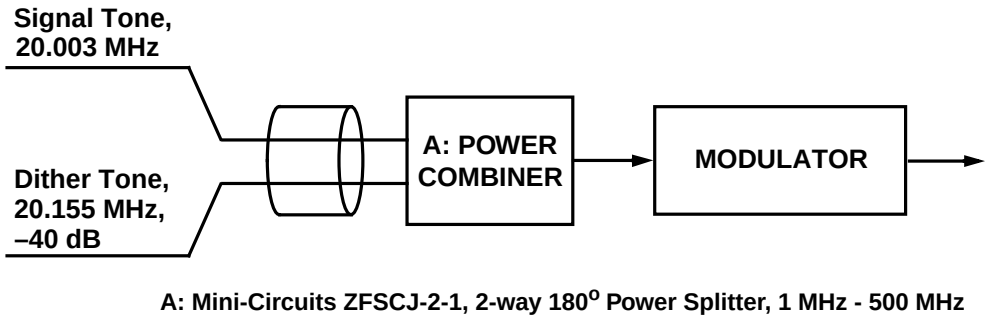


Figure 7.8: Application of out-of-band sinusoidal dither.

Out-of-band sinusoidal dither was applied at the input of the experimental modulator to improve its low-input level performance. In the presence of a –40 dB dither signal at 20.155 MHz, the modulator is always being exercised by an active signal, regardless of the actual input signal level. Consequently, the magnitude of the tones at dc and $f_s/2$ is greatly reduced. The dither signal is removed by the ensuing decimation filter, and so has no impact upon the performance of the modulator other than reducing the dynamic range by approximately 1 dB. Figure 7.8 illustrates how a –40 dB dither tone was applied to the input of the modulator using a power combiner. In an actual radio environment, it is likely that out-of-band signals will provide the necessary dithering.

Plots of the SNR and SNDR versus input signal level when dither is used are shown in Figure 7.9. The experimental prototype is seen to achieve a measured dynamic range of 75 dB for a signal bandwidth of 200 kHz centered at 20 MHz and a peak signal-to-noise ratio of 72 dB. The peak signal-to-noise plus distortion ratio is 70 dB. The measured total passband noise of the prototype is –77 dB. The dynamic range of the prototype modulator is limited by circuit noise, not quantization noise. Therefore, by holding the sampling frequency constant and reducing the signal bandwidth from 200 kHz to 100 kHz, the dynamic range is increased by 3 dB to 78 dB. Similarly, for a 30-kHz passband, as required in IS-54 digital cellular systems, the dynamic range exceeds 80 dB.

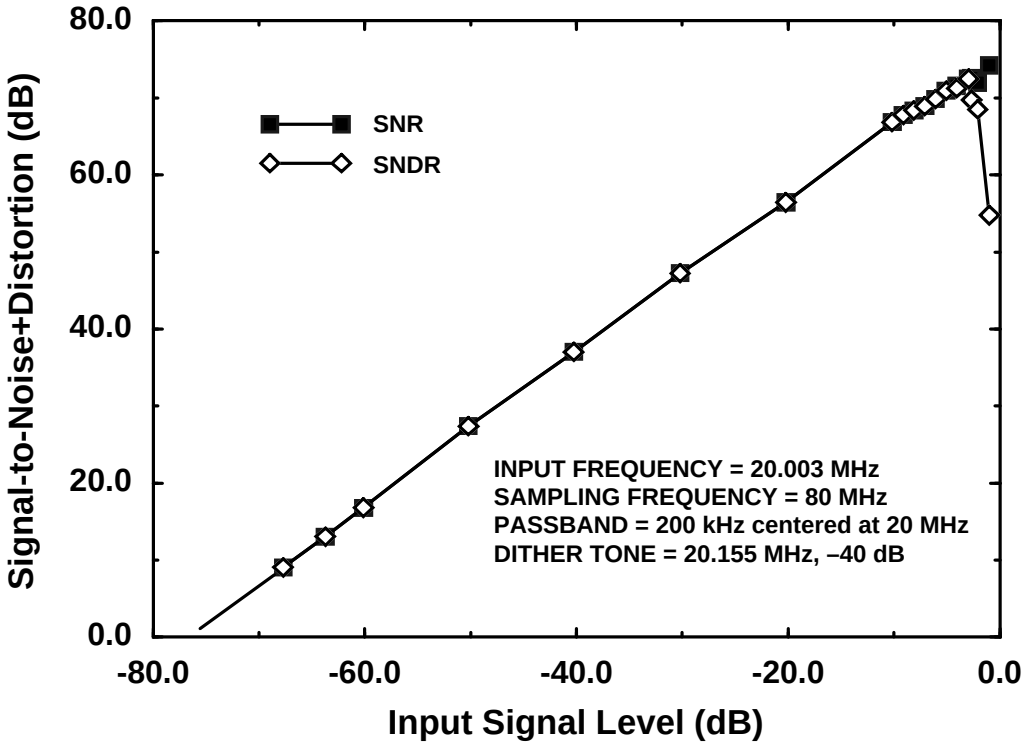


Figure 7.9: Measured SNR and SNDR when dither has been applied to the experimental modulator.

7.3.2 Intermodulation Distortion

The linearity of the experimental prototype has also been evaluated by subjecting the modulator to a two-tone intermodulation test. When two sinusoids with frequencies ω_1 and ω_2 are applied to the input of the modulator, nonlinearities in the system give rise to harmonics of the input signals, as well as additional intermodulation (IM) components that are the result of mixing between the original sinusoids and their harmonics [110]. Of the large number of IM terms, those at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are particularly problematic because, for a certain range of frequencies, they will fall within the signal passband where they cannot be suppressed by filtering. This effect is illustrated in Figure 7.10.

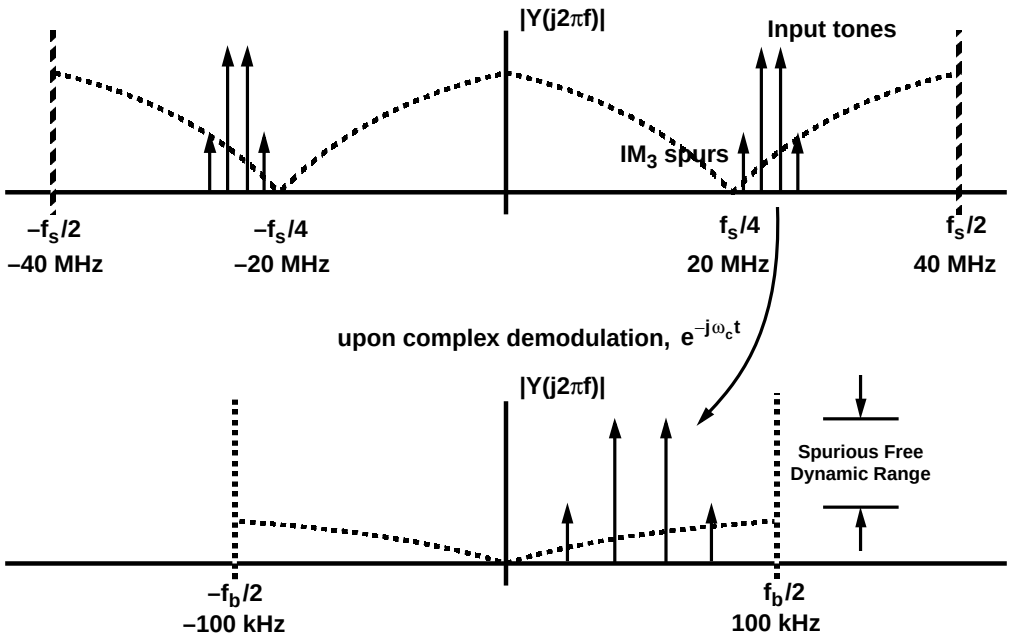


Figure 7.10: Intermodulation spurs arising from third-order nonlinearities in the modulator.

When two tones that are approximately 8 dB below the overload point are applied to the input of the prototype modulator, it can be seen in Figure 7.11(a) that the third-order intermodulation products are suppressed by approximately 69 dB. The skirts around the input tones appear to be artifacts of the high phase noise of the signal generators. This is demonstrated in Figure 7.11(b), which illustrates that when one of the signal generators is replaced by a low phase noise source, the skirt around the signal disappears. The third-order intermodulation products disappear as well, but only because it was necessary to reduce the output level from the low phase noise source to prevent its own distortion from obscuring the intermodulation spurs.

7.4 Summary

An experimental implementation of the two-path, $f_s/4$ modulator described in Chapters 5 and 6 has demonstrated the capability to digitize signals in a 200-kHz passband centered

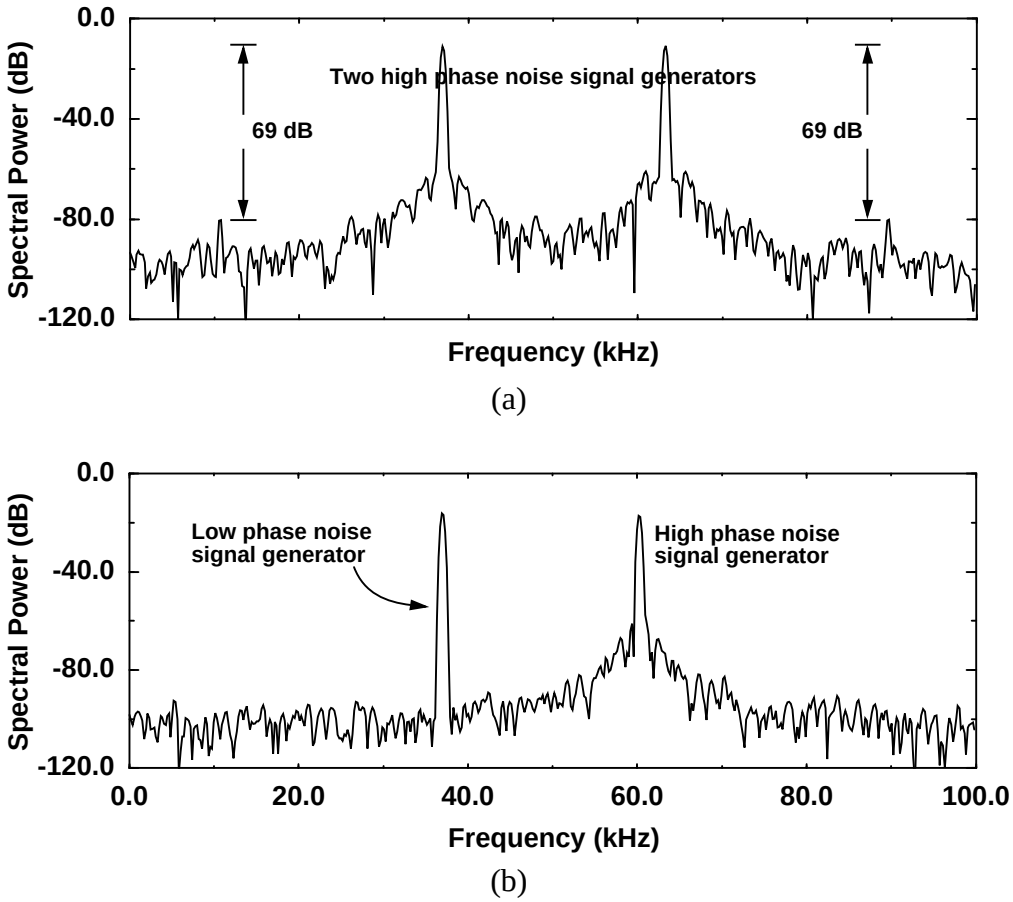


Figure 7.11: Measured two-tone test results for (a) two high phase noise signal sources, and (b) one low phase noise source and one high phase noise source.

at 20 MHz with 75 dB of dynamic range. Measured results for this prototype circuit are summarized in Table 7.1. The measurement results also indicate that the mirror signal inherent to the two-path architecture is suppressed by at least 42 dB, which is considerably better than the 25 dB required by many applications. The experimental prototype was found to suffer from increasing levels of harmonic distortion and a higher level of total passband noise as the input signal level was decreased. Experimental evidence suggests that incomplete, nonlinear settling in the amplifiers causes mixing of tones at dc and $f_s/2$ with the signal in the passband centered at $f_s/4$. Out-of-band sinusoidal dither has been

Parameter	Value
Sampling Speed	**80 MHz**
Passband	**200 kHz centered at 20 MHz**
Oversampling ratio	**200**
Dynamic range	**75 dB**
Peak SNR/SNDR	**72 dB/70 dB**
Supply Voltage	**3.3 V**
Power dissipation	**49 mW – Modulator,** **23 mW – Clock generator**
Technology	**0.6-μm single-poly, triple-metal CMOS**
Active Area	**1.3 mm × 2.1 mm**

Table 7.1: Performance summary of the prototype, two-path modulator.

shown to be an effective remedy for this problem. The phenomenon of tones at dc and $f_s/2$ is not unique to the two-path architecture. Because these tones can occur in many classes of modulators, they pose a hazard to any modulator that centers the signal passband at $f_s/4$.

Chapter 8 *Conclusion*

8.1 Summary

To meet the anticipated requirements imposed by the myriad of next-generation networks for wireless communications, substantial effort is currently being devoted to the development of integrated receivers that are compatible with multiple standards. The investigation of this design space involves tradeoffs between factors such as receiver dynamic range, power dissipation and system linearity. In addition, digitization in the signal path is rapidly becoming a necessity because the emerging digital cellular standards encompass bandwidth-efficient modulation schemes, as well as compression, error correction, and multipath equalization or spread spectrum techniques. Thus, receiver architectures are evolving towards an integrated digital solution in which the RF signal is translated down to a low intermediate frequency or to baseband before being digitized and processed.

This research has studied the challenges involved in implementing a bandpass A/D conversion in the receiver signal path. Bandpass sigma-delta modulation is proposed as the method of choice because oversampled bandpass converters robustly digitize the types of high-frequency, narrowband signals that arise in radios and cellular systems. Furthermore, such converters achieve a large dynamic range without requiring trimming or other steps incompatible with a standard VLSI process.

A number of contributions have resulted from this research. The design of bandpass modulators has been explored with an emphasis on improving their performance at the high sampling speeds (tens of MHz) necessary for wireless applications. A fourth-order $f_s/4$ modulator has been designed to suppress inband quantization noise by at least 90 dB in a 200-kHz passband centered at 20 MHz. An analysis presented herein shows that the

dynamic range of such a modulator is profoundly influenced by incomplete settling of the amplifier outputs if it is implemented using conventional switched-capacitor biquadratic circuits. As one means of reducing the burden imposed upon the amplifiers, this dissertation proposes a new two-path architecture for a fourth-order, $f_s/4$ modulator that is more tolerant of analog circuit limitations at high sampling speeds than conventional implementations. Nonideal effects relating to this two-path architecture have been described and analyzed. In particular, it is shown that random timing jitter results in an increase of inband noise, while systematic timing errors and path mismatch both result in an incomplete mirror signal suppression. The stability of the new two-path architecture has also been studied through behavioral simulations and is seen to be sensitive to specific implementation issues in a manner that is not reflected in the second-order lowpass architecture from which the bandpass topology has been derived. Fortunately, for the specific circuit topology chosen in this work, the two-path modulator remains stable for a wide range of overload conditions provided that capacitor matching is good to approximately 1%, which can be readily achieved.

An experimental prototype of the proposed two-path, $f_s/4$ modulator has been designed and fabricated in a 0.6-μm, single-poly, triple-metal CMOS process through the MOSIS service. Two interleaved paths clocked at 40 MHz digitize a 200-kHz bandwidth signal centered at 20 MHz with 75 dB of dynamic range while suppressing the undesired mirror image signal by 42 dB. At low input signal levels, the mixing of spurious tones at dc and $f_s/2$ with the input appears to degrade the performance of the modulator; out-of-band sinusoidal dither is shown to be an effective means of avoiding this degradation. The experimental modulator dissipates 72 mW from a 3.3-V supply. The passband center frequency of this prototype represents an improvement by roughly a factor of 6 over previously reported $f_s/4$ modulators that have a comparable dynamic range and were implemented in CMOS.

A noise analysis of the experimental prototype reveals that its noise floor is dominated by a combination of amplifier noise and thermal noise from the switches. It has been discovered that the amplifier noise in the first-stage path filter is shaped to have a maximum

spectral density in the signal band centered at $f_s/4$. If this hazardous noise amplification is accounted for, the measured dynamic range of the experimental prototype is seen to lie within 2 dB of that predicted by hand analysis.

8.2 Suggestions for Further Research

8.2.1 Cascaded Bandpass Modulators

The research into high-speed, bandpass, oversampled analog-to-digital conversion described in this dissertation has focused on implementing analog-to-digital converters that digitize signals with bandwidths between 30 kHz and 200 kHz centered at intermediate frequencies (IF) as high as 20 MHz. Such converters would be useful in digitizing the first IF of traditional FM receivers with carriers around 100 MHz, or the second IF in cellular telephony and wireless data terminals with carriers between 900 MHz and 2 GHz. Hitherto, sampling rate limitations and architectural choices in the design of antecedent modulators [54]-[56], [67]-[70] have hindered the digitization of signals with bandwidths much larger than 200 kHz. However, new spread-spectrum standards such as IS-95 specify signal passbands with a 1.25-MHz bandwidth. Therefore, it is of interest to extend the passband bandwidth to accommodate the different and competing standards that currently proliferate in the wireless market. Cascaded bandpass structures are as proposed a possible method by which high-bandwidth signals can be digitized.

In bandpass modulators, the passband bandwidth is limited by two related factors. As described in Section 3.3.1, the passband is often restricted to lie at one-quarter of the sampling frequency because comparatively simple analog circuits can then be used to implement the modulator. Moreover, one class of $f_s/4$ bandpass topologies can easily be derived from lowpass prototypes with a simple dc-to-$f_s/4$ transformation, (3.23). Thus, once the IF location has been determined, the sampling frequency is constrained as well. This in turn limits the maximum passband bandwidth because the modulator must digitize the signal with a minimum acceptable oversampling ratio. Otherwise, the modulator will not achieve the wide dynamic range (>70 dB) needed to reject adjacent-channel interferers. Previous

high-speed designs [54], [70] have employed fourth-order topologies that require oversampling ratios of 100 to 200 to digitize 200-kHz signal bandwidths with a dynamic range on the order of 70 to 80 dB.

Wider passbands can be digitized by increasing either the sampling frequency or the order of the modulator. In 0.6-μm CMOS technologies, it seems unlikely that the effective sampling frequency of switched-capacitor circuits can be extended much beyond 100 MHz without compromising the settling behavior of the circuits. This remains true even if the modulator is implemented with time-interleaved circuits as described in this dissertation. Furthermore, it is not clear that the passband bandwidth can be increased significantly simply by sampling at a higher frequency. For example, if the modulator sampling frequency is increased from 80 MHz to 100 MHz, and the oversampling ratio is held constant at 200, the signal bandwidth increases only from 200 kHz to 250 kHz. An increase in the sampling frequency also necessitates a change in the IF location, which is a system parameter that might not be under the control of the circuit designer. Therefore, to increase the passband bandwidth, it is necessary to increase the order of the modulator.

Higher-order modulators can be designed without compromising the stability of the loop by cascading lower-order stages in a manner similar to lowpass structures. Several low speed implementations have already proven the feasibility of this approach [68], [69], and simulations have shown that a sixth-order modulator comprised of a fourth-order and second-order cascade can achieve a dynamic range in excess of 90 dB with an oversampling ratio of only 64 [118]. Extrapolating from these results, by utilizing an eighth-order modulator comprised of a 4-4 cascade, it may be possible to digitize signals with a 1.25-MHz bandwidth centered at 20 MHz with a sampling frequency of only 80 MHz and an effective oversampling ratio of 32. Time-interleaving can also be exploited in a cascaded modulator to relax the demand upon the analog circuit constituents.

Cascaded architectures also have the benefit of providing the designer with additional degrees of freedom. In the design of both lowpass and bandpass modulators, in order to achieve the maximum dynamic range for a given supply voltage and minimum power dissipation, it is important to adjust various system gains so as to scale the signal swings at

internal nodes within the modulator [98]. In a fourth-order bandpass modulator, without such scaling, the signal swing at the output of the first resonator can be as large as twice the feedback reference level. This large signal swing can cause linearity problems, especially as the supply voltage is reduced, as the op amps move out of their linear regions. This signal swing cannot be significantly scaled without also reducing the feedback reference voltages, and thereby reducing the full-scale input range of the modulator. As a consequence, the input-referred noise floor must be lowered to achieve a given dynamic range, and this requires a disproportionate increase in current levels, and, therefore, power dissipation [98]. In a cascaded modulator architecture, the additional degrees of freedom available with respect to both resonator gains and the noise-mixing paths allow considerable flexibility in scaling the signal swings at internal nodes.

Finally, as the experimental evidence as presented in this dissertation shows, the performance of fourth-order, single-loop bandpass modulators can be degraded at low input-signal levels. As the input signal drops approximately 40 dB below full scale in the experimental prototype, the passband noise energy begins to increase and tones harmonically related to the input signal begin to appear in the passband. It is postulated that this degradation is the result of intermodulation distortion between the signal at $f_s/4$ and families of spurious noise tones at dc and $f_s/2$. These tones at dc and $f_s/2$ become apparent only as the input signal is reduced. They are not evident for inputs near full scale, and for large signals the measured passband noise is consistent with the performance being limited by electronic noise in the modulator. It appears that out-of-band sinusoidal dither introduced at the modulator input can be used to circumvent the anomalous performance at low signal levels by ensuring that the modulator always sees an active input. However, there is currently no clear understanding of the phenomena, other than that it appears to be related to coloration in the output spectrum. Because for lowpass modulators quantization noise in cascaded architectures is known to be less correlated with the input than in single-loop architectures, it is thought that cascaded bandpass architectures might suppress spurious noise tones at dc and $f_s/2$. Consequently, a sixth- or eighth-order cascaded bandpass mod-

ulator may be tolerant of more circuit nonlinearities than a fourth-order, single-loop modulator.

8.2.2 Alternative Multipath Modulator Architectures

The exploitation of *N*-path principles in high-speed modulator design is not limited to the implementation of two-path, $f_S/4$ architectures. This approach can be generalized, and alternative architectures can be derived that center the passband at frequencies other than $f_S/4$. As one example, an $f_S/3$ modulator can be constructed by interleaving three independent, second-order, lowpass modulators in the manner depicted in Figure 8.1. Each modulator is clocked on a separate phase of a three-phase, non-overlapping clock, and the outputs are interleaved. An output spectrum from a behavioral simulation is shown in Figure 8.2. It is interesting to note that the quantization noise at the output of the interleaved array is suppressed around dc as well as $f_S/3$. Since the noise transfer function has a zero at dc, tones at dc are suppressed by the action of the modulator. Consequently, there is less potential for distortion to be introduced into the signal passband by the "mixing" of tones at dc with the input signal at $f_S/3$, which was identified as a significant hazard in this dissertation. However, this property does not imply that high-level tones cannot be generated at alternate frequencies, such as near 10 MHz, and still mix into the passband through distortion mechanisms.

One advantage of using a three-path, $f_S/3$ modulator architecture is that such an architecture permits the digitization of IF signals centered as high as 20 MHz while the critical circuit blocks are clocked at only 20 MHz. The architecture does not rely on subsampling principles to "mix" the high-frequency passband down to a lower frequency before digitization occurs. Therefore, the dynamic range is not degraded by aliasing of wideband noise. Thus, a three-path, $f_S/3$ modulator can potentially digitize signals centered at the same frequency and with similar performance as the two-path $f_S/4$ modulator demonstrated in this thesis, but at a lower power dissipation. However, two problems are immediately apparent with this approach. First, it will be more difficult to guarantee that the mirror image is suppressed by greater than 40 dB given that three paths, instead of two,

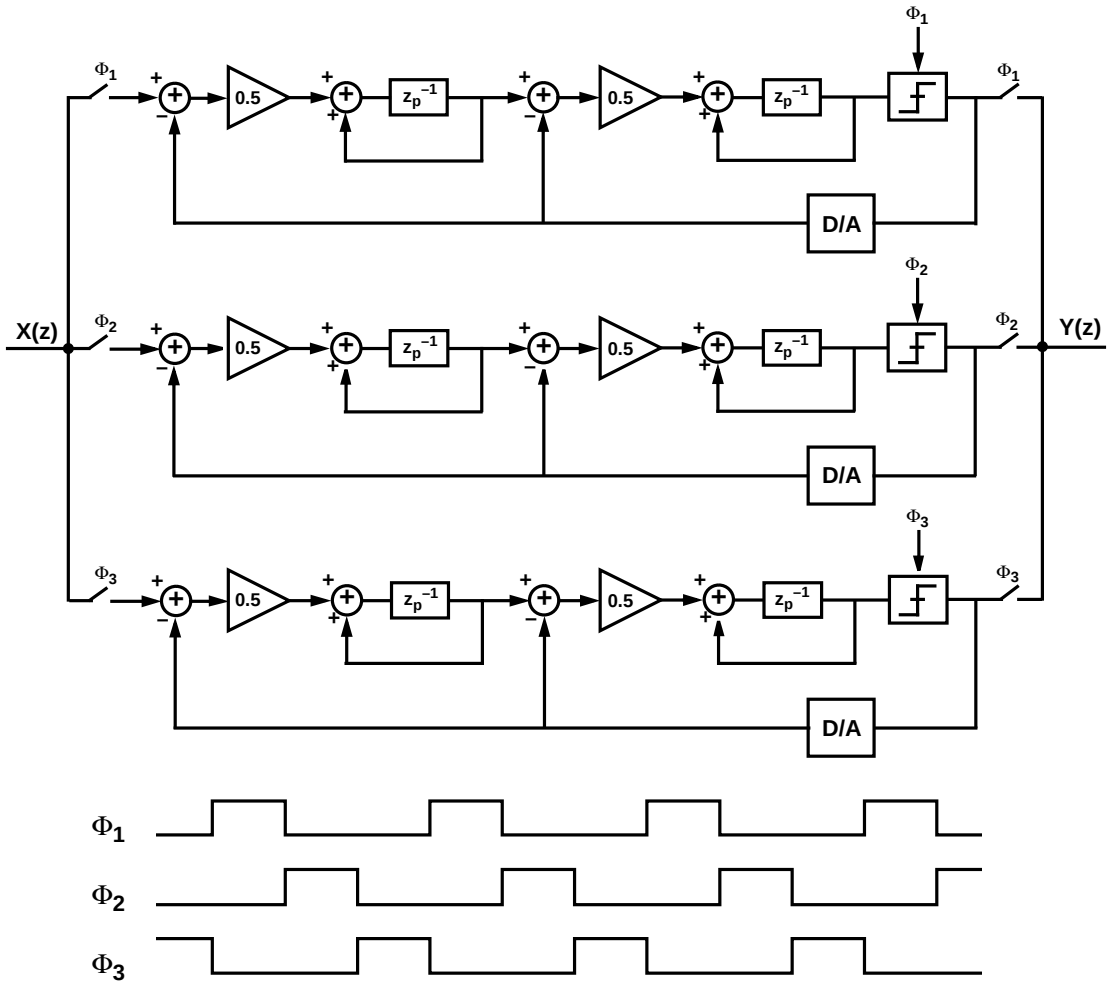


Figure 8.1: Block diagram of a three-path, $f_s/3$ modulator.

contribute to the overall mismatch in the modulator. Secondly, signal-independent errors such as clock feedthrough will result in a tone in the middle of the passband rather than at an out-of-band location. However, these artifacts are analogous to those introduced by interleaving arrays of Nyquist-rate A/D converters. Therefore, it is conceivable that these types of errors can be detected and calibrated out of the array in either the analog or the digital domain as has been demonstrated in the case of Nyquist-rate A/D converters [119], [120].

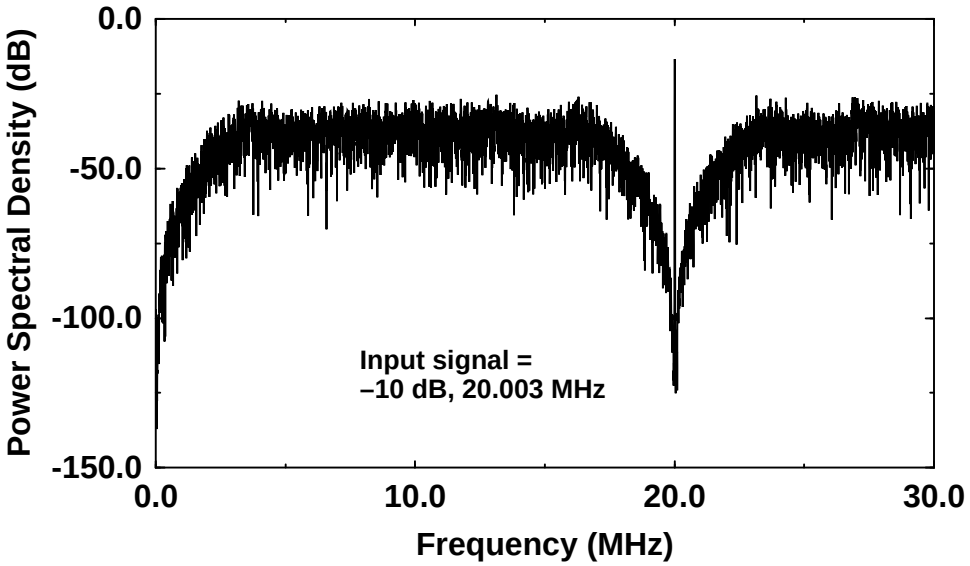


Figure 8.2: Undecimated spectrum of a three-path, $f_s/3$ modulator.

Appendix A The Design of a Fourth-Order, $f_s/6$ Modulator

This appendix illustrates the design procedure described in Section 3.3.4.2 for synthesizing a noise transfer function that meets the causality, (3.48), and gain, (3.49), requirements for an f_s/X bandpass modulator. As an example, the design flow is used to design a fourth-order, $f_s/6$ Butterworth noise transfer function with an out-of-band gain of 1.8. MATLAB is used extensively to circumvent the tedium associated with the requisite algebraic transformations, which map a continuous-time Butterworth filter into the *z*-domain by means of the bilinear transform (3.34); the details of this filter design process can be found in [18].

A.1 Noise Transfer Function Design Flow

In the following steps, the MATLAB *butter* function is used to design a fourth-order, Butterworth bandstop filter. Similar methodology can be used to design Chebyshev, elliptical, or other special classes of discrete-time filters.

(1) Choose the order and the out-of-band gain of the NTF. In this example, the filter is fourth-order and will have a maximum out-of-band gain of 1.8.

(2) Two design parameters, ω_o and Δ, are used in this design flow to synthesize a bandstop filter in MATLAB using the *butter* function. ω_o is approximately equal to the center frequency of the bandstop region; the frequency axis is normalized to $-\pi$ to π, which corresponds to $-f_s/2$ to $f_s/2$. Δ is correlated with the width of the bandstop region, so it is chosen to be some small fraction of the total normalized sampling bandwidth, 2π. In this example, the bandstop region is centered at $f_s/6$, so $\omega_o = \pi/3$, and Δ is chosen initially to equal 0.1π.

(3) Design the filter using the *butter* function in MATLAB. A transcript for the design of a fourth-order, $f_s/6$ noise transfer function is shown below. The out-of-band gain is 1.8, $\omega_o = \pi/3$, and $\Delta = 0.1\pi$.

```
>> gain = 1.8;
>> order = 4;
>> wo = pi/3;
>> delta = 0.1*pi;
>> wn = [wo-delta wo+delta]/pi;
>> [b,a] = butter(order/2,wn,'stop');
>> b = b*gain;
>> [h,w] = freqz(b,a);
>> plot(w,abs(h))
>> b
  b =
      1.1501   -2.4186    3.5717   -2.4186    1.1501
  a =
      1.0000   -1.6524    1.8494   -1.0349    0.4128
```

With the given design parameters, the *butter* function returns

$$NTF(z) = \frac{b_1 z^{-1} + b_2 z^{-2} + \ldots + b_N z^{-N}}{a_o + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_N z^{-N}}$$

$$= \frac{1.1501 - 2.4186 z^{-1} + 3.5717 z^{-2} - 2.4186 z^{-3} + 1.1501 z^{-4}}{1 - 1.6524 z^{-1} + 1.8494 z^{-2} - 1.0349 z^{-3} + 0.4128 z^{-4}} \quad . \qquad \text{(A.1)}$$

(4) Look at the b_1 coefficient. If $b_1 \neq 1$, adjust Δ and resynthesize the filter until $b_1 = 1$. This insures that the causality requirement, (3.48), on $NTF(z)$ is satisfied.

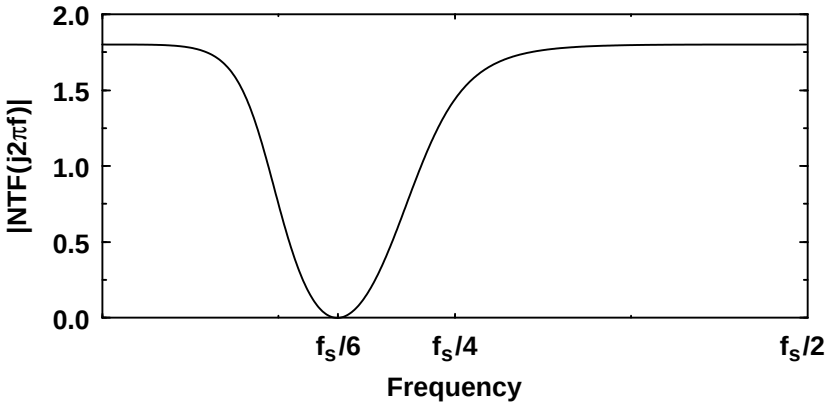


Figure A.1: Magnitude response of the fourth-order, $f_s/6$ noise transfer function, (A.3), designed iteratively using MATLAB.

(6) After meeting the causality requirement, the zeros of $NTF(z)$ must be positioned at the desired noise null. The zeros can be manipulated independently of b_1 by adjusting ω_o. Usually, only a few iterations are necessary before the numerator of $NTF(z)$ is correctly specified. For a fourth-order, Butterworth, $f_s/6$ noiseshaping function, the zeros of $NTF(z)$ lie on the unit circle at $z = \cos(\pi/3) \pm j\sin(\pi/3)$. Therefore the numerator of $NTF(z)$ is

$$N(z) = \left[1 - \left(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}\right)z^{-1}\right]^2 \times \left[1 - \left(\cos\frac{\pi}{3} - j\sin\frac{\pi}{3}\right)z^{-1}\right]^2 \qquad (A.2)$$
$$= 1 - 2z^{-1} + 3z^{-2} - 2z^{-3} + z^{-4} .$$

In this example, after iterating through steps 5 and 6 the design parameters Δ and ω_o are found to be $\Delta = .13009\pi$ and $\omega_o = 0.34827\pi$. The final fourth-order, $f_s/6$ noise transfer function that result from this design flow is

$$NTF(z) = \frac{1 - 2z^{-1} + 3z^{-2} - 2z^{-3} + z^{-4}}{1 - 1.4514z^{-1} + 1.4583z^{-2} - 0.7709z^{-3} + 0.3195} . \qquad (A.3)$$

The magnitude response of (A.3) is shown in Figure A.1.

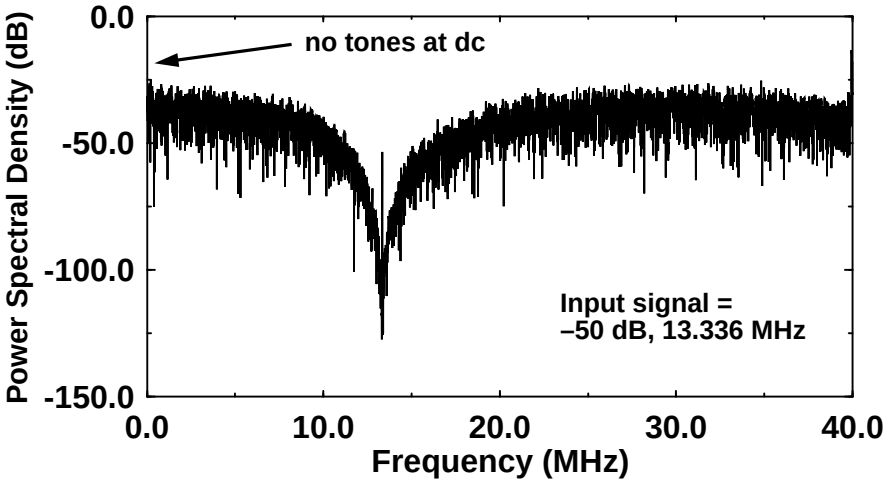


Figure A.2: Magnitude response of a fourth-order, $f_s/6$ modulator with a Butterworth noise transfer function designed iteratively using MATLAB.

A.2 $f_s/6$ Modulator Design

Once the noise transfer function has been found, the design of a feedback modulator that implements the desired NTF is a matter of algebraic manipulation of $NTF(z)$. The feedback filter, $F(z)$, is chosen to be 1, so from (3.46), the transfer function of the forward path filter, $A(z)$, is found to be

$$A(z) = \frac{0.5486z^{-1} - 1.5417z^{-2} + 1.2291z^{-3} - 0.6805z^{-4}}{1 - 2z^{-1} + 3z^{-2} - 2z^{-3} + z^{-4}} \quad . \tag{A.4}$$

Figure A.2 depicts the undecimated output spectrum of an $f_s/6$ modulator with $A(z)$ as given by (A.4) and $F(z) = 1$. The spectrum is seen to be substantially similar to the spectrum shown in Figure 3.24(a), which is the output of an $f_s/6$ modulator designed using the Constantinides lowpass-to-bandpass transformation. In both cases, no tones are visible at dc for the input signal shown. In Figure A.3, the plots of signal-to-quantization noise versus input signal level indicate that the modulator is not extremely sensitive to the exact value of the coefficients of $A(z)$, which suggests the possibility that this design may be suitable for VLSI implementation. However, the SNR peaks at a level well below 0 dB, so

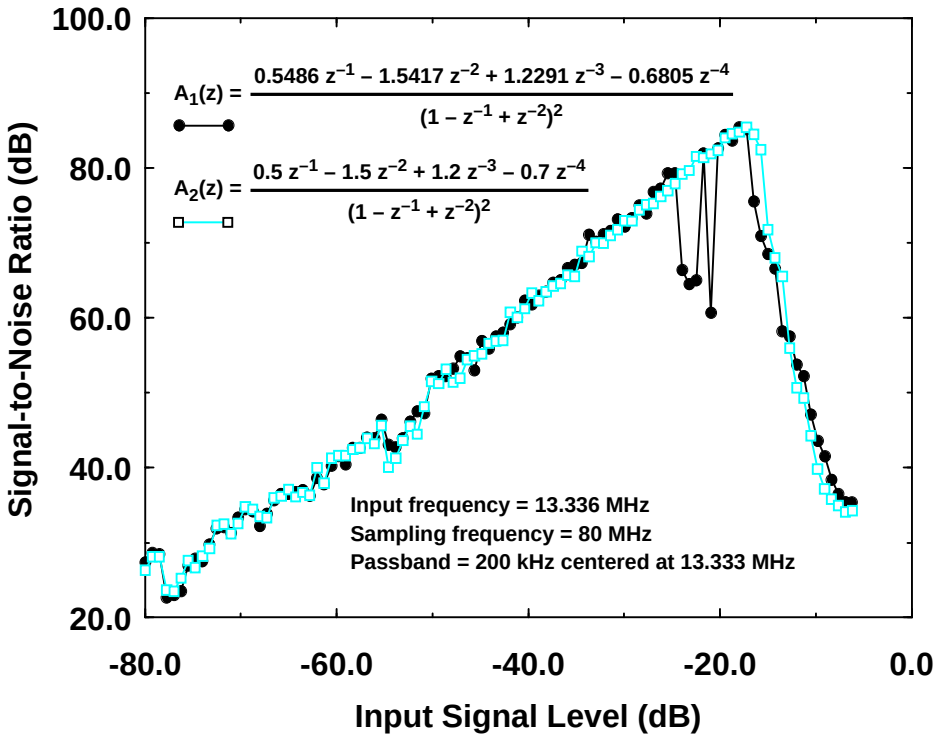


Figure A.3: SNR vs. Input Signal Level of a fourth-order, $f_S/6$ modulator with a Butterworth noise transfer function.

the use of a different noise transfer function might improve the modulator's dynamic range. In addition, the modulator is seen in Figure A.3 to exhibit anomalous SNR degradation when the input is approximately –25 dB. Unfortunately, these types of pathologies cannot be predicted for a particular modulator architecture with the analysis and design framework established in this dissertation. In the absence of analytical methods, only extensive behavioral simulations can reveal gross departures from the expected performance of a particular modulator design.

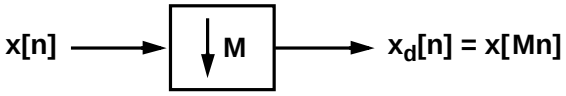
Appendix B N-Path Filter Analysis Using Multirate Signal Processing

This appendix derives the transfer function for an *N*-path filter using the framework established for the analysis of multirate discrete-time signal processing [111], [112]. The term *multirate* refers to the fact that sampling rate is not constant within the system. Rather, there are downsamplers and upsamplers embedded within the system. It is first necessary to derive the transform relationships for these operations before an overall transfer function for the *N*-path filter can be developed. The essential relationships are established in the following sections, and a more detailed treatment can be found in [111].

The analysis of *N*-path filters bears substantial similarity to the analysis of time-interleaved A/D converter banks [113], [114], quadrature mirror filtering [115], [116], and subband decomposition [117]; these related subjects can provide an additional perspective on the subject of *N*-path filtering that lies beyond the scope of this dissertation.

B.1 Downsampling

A downsampler, also called a decimator, is depicted in Figure B.1 with the downsampling ratio given by the factor shown in the box, *M*. The output sequence, $x_d[n]$, is derived from the input sequence, $x[n]$, with the relationship



M-fold downsampler

Example with M = 2

n	0	1	2	3	4	5	6	7	...
x[n]	3	2	–1	0	9	7	2	6	...
$x_d[n]$	3	–1	9	2	...				

Figure B.1: Block diagram of an M-fold downsampler with an example of downsampling by a factor of two on an input signal, $x[n]$.

$$x_d[n] = x[Mn] = x_c(MnT) . \tag{B.1}$$

From (B.1) it is clear that $x_d[n]$ can be obtained by taking every M^{th} sample of the discrete-time sequence, $x[n]$, or by sampling the original continuous-time signal, $x_c(t)$, at $1/(MT)$ instead of $1/T$.

It can be shown that the output of the decimator can be represented in the z-domain as [111]

$$X_d(z) = \frac{1}{M} \sum_{k=0}^{M-1} X(z^{1/M} e^{-j2\pi k/M}) . \tag{B.2}$$

where $X(z)$ is the z-transform of $x[n]$. If the input sampling rate, $1/T$, is normalized to unity, then the spectrum of $x_d[n]$ is found by substituting $z = e^{j\omega}$ into (B.2), which yields:

$$X_d(e^{j\omega}) = \frac{1}{M} \sum_{k=0}^{M-1} X\left(e^{j\left(\frac{\omega}{M} - \frac{2\pi k}{M}\right)} \right) . \tag{B.3}$$

Thus, as shown in Figure B.2, the spectrum of $x_d[n]$ consists of M frequency-scaled and shifted copies of the spectrum of $x[n]$ that are centered at multiples of 2π. The spectra, $X(e^{j\omega})$ and $X_d(e^{j\omega})$, are both periodic in 2π.

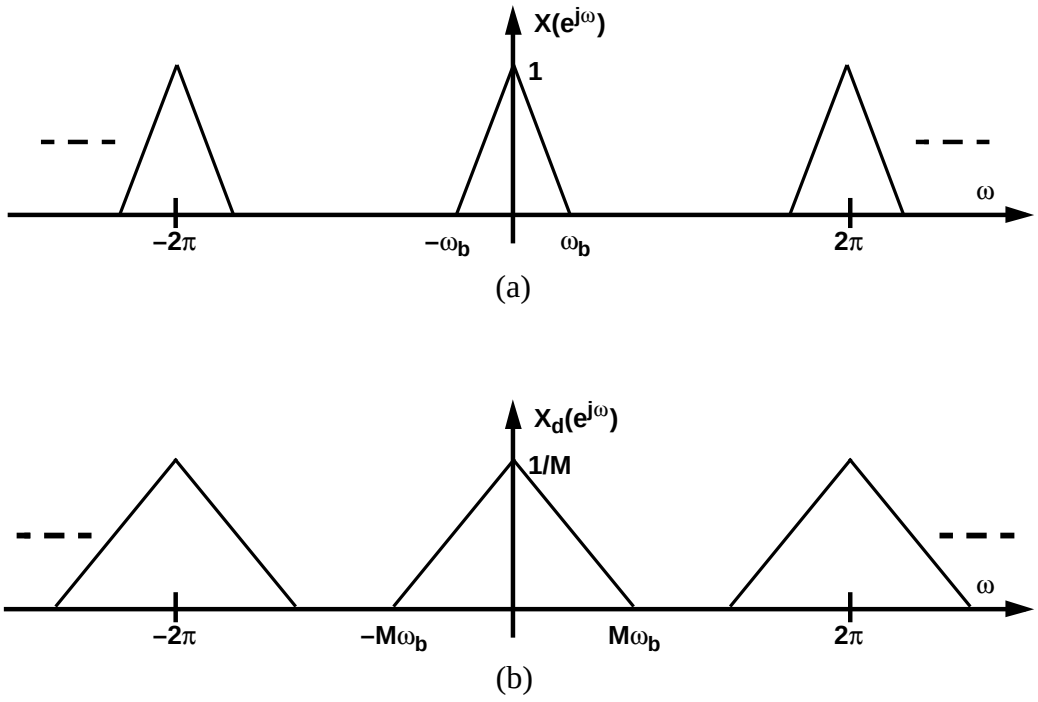


Figure B.2: Spectrum of (a) $x[n]$ and (b) $x_d[n]$ with the input sampling rate, $1/T$, normalized to unity.

B.2 Upsampling

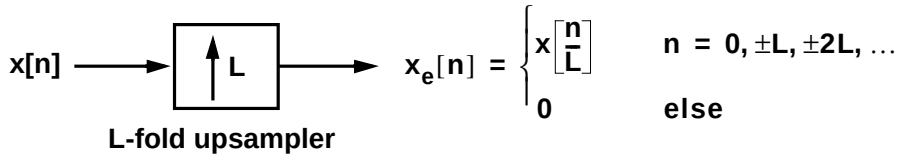
The sampling rate of a discrete-time signal can be increased by applying the signal to an upsampler, as shown in Figure B.3. The input-output relationship of the upsampler is

$$x_e[n] = \begin{cases} x\left[\frac{n}{L}\right] & n = 0, \pm L, \pm 2L, \ldots \\ 0 & \text{else} \end{cases} . \tag{B.4}$$

From (B.4) it is seen that upsampling involves inserting $L - 1$ zeros between the samples of the input sequence, $x[n]$.

In the z-domain, it can be shown that the output of the upsampler is [111]

$$X_e(z) = X(z^L) . \tag{B.5}$$



Example with L = 2

n	0	1	2	3	4	5	6	7	...
x[n]	3	2	–1	0	9	7	2	6	...
$x_e[n]$	3	0	2	0	–1	0	9	0	...

Figure B.3: Block diagram of an L-fold upsampler with an example of upsampling by a factor of two on an input signal, $x[n]$.

Once again, normalizing the input sampling rate, $1/T$, to unity, the frequency spectrum of the interpolated signal, $x_e[n]$, is found by substituting $z = e^{j\omega}$ into (B.5):

$$X_e(e^{j\omega}) = X(e^{j\omega L}) . \tag{B.6}$$

The effect of interpolation in the frequency domain is to compress the original frequency spectrum of $X(e^{j\omega})$ from $(-\pi, \pi)$ to $(-\pi/L, \pi/L)$ as illustrated in Figure B.4. As a consequence, the spectrum of the interpolated signal, $X_e(e^{j\omega})$, contains $L - 1$ frequency-scaled replicas of the basic prototype spectrum, $X(e^{j\omega})$, between $-\pi$ and π. This frequency compression is a dual of the aliasing property exhibited by downsamplers.

B.3 *N*-Path Filter Analysis

With the principles of downsampling and upsampling established in the previous two sections, the N-path filter shown in Figure 5.1 and repeated in Figure B.5(a) can be represented as a multirate discrete-time system, as shown in Figure B.5(b). Recall that in Figure B.5(a), z_p corresponds to the z variable of a single path; z_p^{-1} is interpreted as a single delay with respect to the path sampling rate. However, in Figure B.5(b), the interleaved

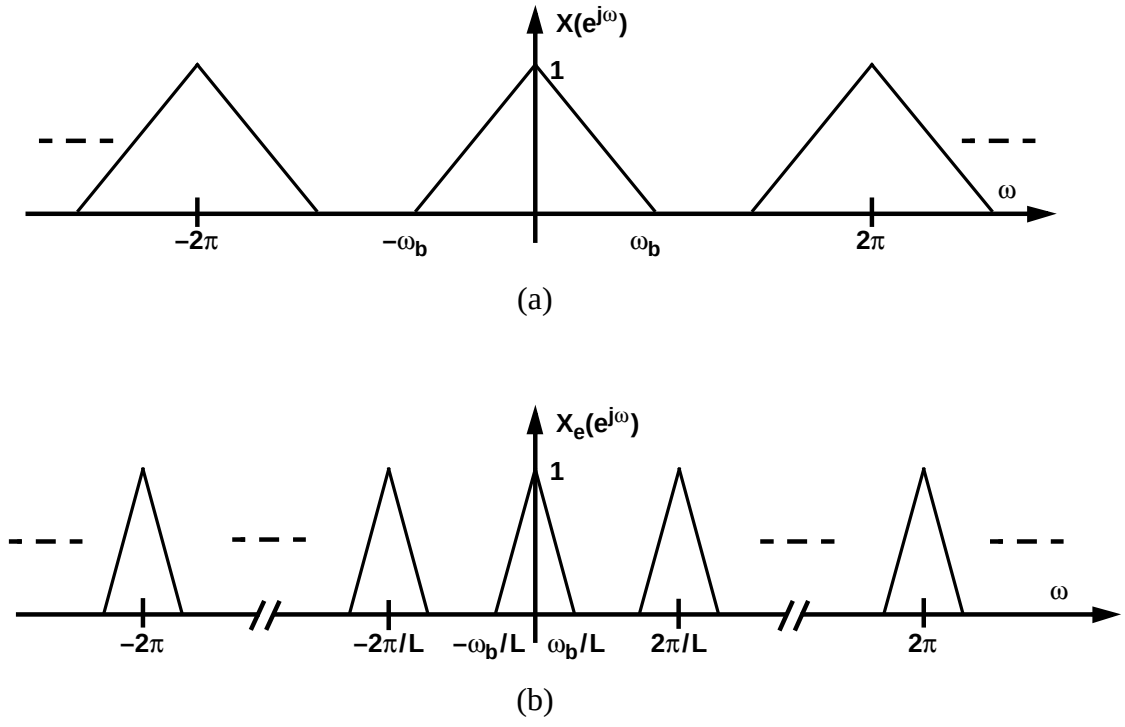
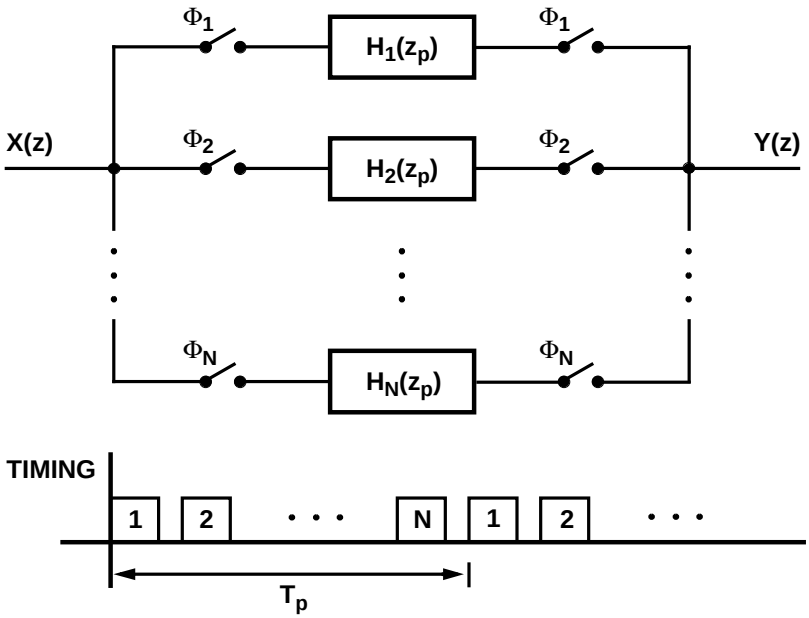


Figure B.4: Frequency spectrum of (a) $x[n]$ and (b) $x_e[n]$.

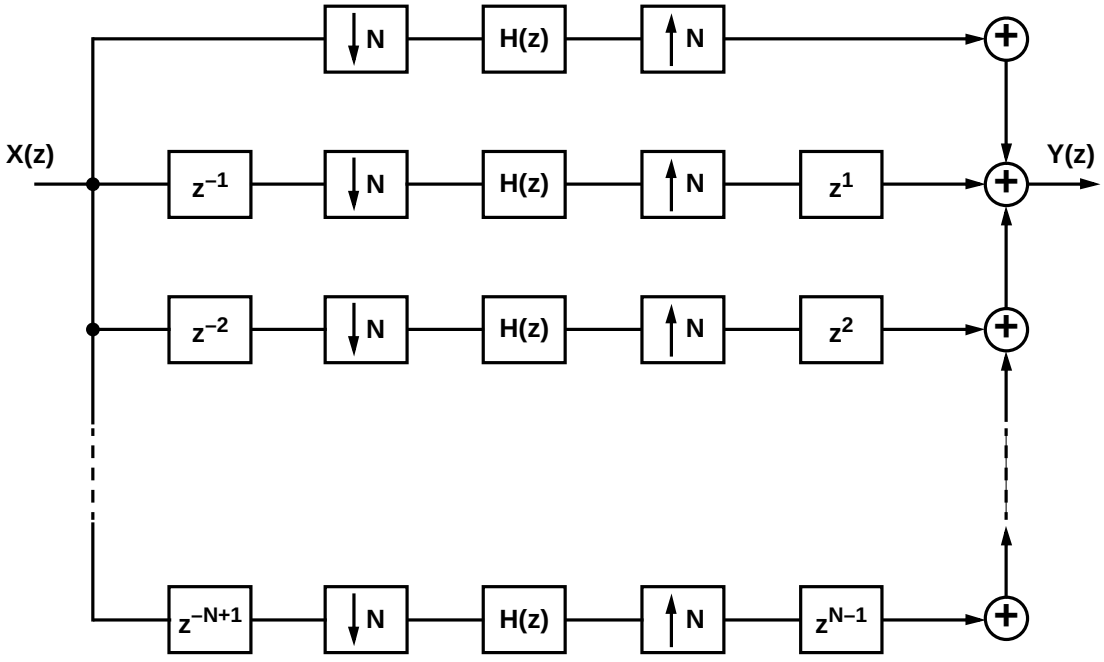
sampling process is represented using a combination of delays and downsamplers that are defined such that they can be referenced to the same z variable. This simplifies the analysis using z-transform methods. The two representations are equivalent.

The N parallel streams are filtered by the path filters, $H_0(z) = H_1(z) = \ldots = H_{N-1}(z) = H(z)$. Following the filtering, the streams are upsampled by a factor of N. The output signal, $Y(z)$, is the sum of the N filtered and shifted streams.

By carefully tracing through Figure B.5(b) and using the z-domain relationships for the downsampler and upsampler, equations (B.2) and (B.5), it can be shown that the output of the filter is



(a)



(b)

Figure B.5: An *N*-path filter represented as (a) interleaved path filters, and (b) a multirate, discrete-time system that can be analyzed in the *z*-domain.

$$Y(z) = \frac{H(z^N)}{N} \sum_{k=0}^{N-1} X(ze^{-j2\pi k/N}) + \frac{H(z^N)}{N} \sum_{k=0}^{N-1} e^{j2\pi k/N} X(ze^{-j2\pi k/N}) + \ldots$$
$$+ \frac{H(z^N)}{N} \sum_{k=0}^{N-1} e^{j2\pi k\frac{N-1}{N}} X(ze^{-j2\pi k/N}) \quad . \tag{B.7}$$

This expression can be written more compactly as

$$Y(z) = \frac{H(z^N)}{N} \left[\sum_{m=0}^{N-1} \sum_{k=0}^{N-1} e^{j2\pi km/N} X(ze^{-j2\pi k/N}) \right] \quad . \tag{B.8}$$

Interchanging the summations with respect to k and m leads to

$$Y(z) = \frac{H(z^N)}{N} \left[\sum_{k=0}^{N-1} \sum_{m=0}^{N-1} e^{j2\pi km/N} X(ze^{-j2\pi k/N}) \right] \quad , \tag{B.9}$$

which can be separated as

$$Y(z) = \frac{H(z^N)}{N} \left[\sum_{k=0}^{N-1} X(ze^{-j2\pi k/N}) \sum_{m=0}^{N-1} e^{j2\pi km/N} \right] \tag{B.10}$$

Finally, making use of the relationship

$$\sum_{m=0}^{N-1} e^{j2\pi km/N} = \begin{cases} N & k = 0, \pm N, \pm 2N, \ldots \\ 0 & \text{else} \end{cases} \quad , \tag{B.11}$$

it is found that

$$Y(z) = \frac{H(z^N)}{N} \left[X(ze^{-j2\pi 0/N}) \cdot N \right] \tag{B.12}$$
$$= H(z^N) \; X(z) \quad ,$$

which is precisely the result stated in equation (5.1).

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